IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 040373/0300

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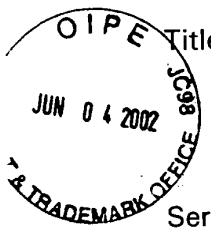
Suler

Applicant: Toshiyuki HIROTA et al.



Title: SEMICONDUCTOR DEVICE WITH HIGH- AND LOW-DENSITY REGIONS OF TRANSISTOR ELEMENTS ON SINGLE SEMICONDUCTOR SUBSTRATE, AND METHOD OF MANUFACTURING SUCH SEMICONDUCTOR DEVICE

Serial No.: 09/741,195

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Art Unit: 2811

PERFECTION OF CLAIM FOR CONVENTION PRIORITY

Commissioner for Patents
Washington, D.C. 20231

Sir:

The benefit of the filing date of the following prior foreign application filed in the following foreign country was requested in a claim for convention priority that was filed on December 22, 2000, where the right of priority provided in 35 U.S.C. §119 was claimed.

In order to perfect that claim, filed herewith is a verified translation of the original foreign application:

Japan Patent Application No. 11-367831 filed December 24, 1999.

Respectfully submitted,

June 4, 2002
Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Japanese Application of

Toshiyuki HIROTA et al.

Japanese Patent Application No.: 367831/1999

Japanese Patent Filing Date: December 24, 1999

for: "METHOD OF MANUFACTURING A CIRCUIT, SEMICONDUCTOR DEVICE"

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks

Washington, D.C. 20231

Sir:

Satoshi YAMAGUCHI residing at 1-18-3-3-104, Utsukushigaoka, Aoba-ku, Yokohama-shi, Kanagawa, Japan, declares:

(1) that he knows well both the Japanese and English languages;

(2) that he translated the above-identified Japanese Application from Japanese to English;

(3) that the attached English translation is a true and correct translation of the above-identified Japanese Application to the best of his knowledge and belief; and

(4) that all statements made of his own knowledge are true and that all statements made on information and belief and believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereof.

May 15, 2002
Date

Satoshi Yamaguchi
Satoshi YAMAGUCHI

(translation)

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this office.

Date of Application: December 24, 1999

Application Number: 367831/1999

Applicant(s): NEC Corporation

September 18, 2000

Commissioner,
Japan Patent Office Kozo OIKAWA (Seal)

Shussho No. Shusshotoku 2000-3074115

[Document Name] Patent Application

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[To] Commissioner, Patent Office

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[Material Name]	Abstract	1

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【Document Name】 Specification

【Title of Invention】 method of manufacturing a circuit, semiconductor device

【Claims】

【Claim 1】 A method of manufacturing a circuit for forming a semiconductor device in which a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density exist on a single semiconductor substrate, is characterized in that;

a gate oxide film is formed on the surface of the high-density region and the low-density region of said semiconductor substrate;

gate electrodes of said transistor elements are formed in a predetermined high density arrangement at said high-density region and in a predetermined low density arrangement at said low-density region, on the surface of the gate oxide film;

a first nitride film having a predetermined thickness is uniformly formed on the surface of said high-density region and said low-density region;

said first nitride film of said low-density region is etched while only said high-density region is masked, therefore said gate oxide film is exposed in gaps between said gate electrodes of said low-density region;

a second nitride film having a predetermined

thickness is uniformly formed on the surface of said high-density region and said low-density region;

an interlayer insulating film with an impurity introduced therein is formed on the surface of said second nitride film;

a void which occurs in the interlayer insulating film disappears by annealing in an atmosphere containing water vapor;

contact holes reaching said semiconductor substrate are formed in said interlayer insulating film by self-alignment in said high-density region with said first nitride film positioned on side of said gate electrodes as an etching stopper;

contact electrodes connected to said semiconductor substrate are formed from the contact holes formed in the interlayer insulating film; and

an interfacial level is recovered by annealing with a forming gas after each portion of said transistor elements is formed.

【Claim 2】

A method of manufacturing a circuit for forming a semiconductor device in which a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density exist on a single semiconductor substrate, is characterized in that;

a gate oxide film is formed on the surface of the high-density region and the low-density region of said semiconductor substrate;

gate electrodes of said transistor elements are formed in a predetermined high density arrangement at said high-density region, and in a predetermined low density arrangement at said low-density region, on the surface of the gate oxide film, after nitride protective films are separately formed on each surface;

a first nitride film having a predetermined thickness is uniformly formed on the surface of said high-density region and said low-density region;

said first nitride film is uniformly etched so that said nitride protective films are exposed at the surface of said gate electrodes and said gate oxide film is exposed in the gap;

a second nitride film having a predetermined thickness is uniformly formed on the surface of said high-density region and said low-density region;

an interlayer insulating film with an impurity introduced therein is formed on the surface of said second nitride film;

a void which occurs in the interlayer insulating film disappears by annealing in an atmosphere containing water vapor;

contact holes reaching said semiconductor substrate

are formed in said interlayer insulating film by self-alignment in said high-density region with said first nitride film positioned on side of said gate electrodes as an etching stopper;

contact electrodes connected to said semiconductor substrate are formed from the contact holes formed in the interlayer insulating film; and

an interfacial level is recovered by annealing with a forming gas after each portion of said transistor elements is formed.

【Claim 3】

A method of manufacturing a circuit for forming a semiconductor device in which a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density exist on a single semiconductor substrate, is characterized in that;

a gate oxide film is formed on the surface of the high-density region and the low-density region of said semiconductor substrate;

gate electrodes of said transistor elements are formed in a predetermined high density arrangement at said high-density region, and in a predetermined low density arrangement at said low-density region, on the surface of the gate oxide film;

a first nitride film having a predetermined thickness

is uniformly formed on the surface of said high-density region and said low-density region;

said first nitride film of said low-density region is etched while only said high-density region is masked, therefore said gate oxide film is exposed in gaps between said gate electrodes of said low-density region;

the exposed gate oxide film is etched, therefore said semiconductor substrate is exposed in gaps between said gate electrodes of said low-density region;

a second nitride film having a predetermined thickness is formed on the surface of the exposed semiconductor substrate;

an interlayer insulating film with an impurity introduced therein is formed on the surface of said second nitride film;

a void which occurs in the interlayer insulating film disappears by annealing in an atmosphere containing water vapor;

contact holes reaching said semiconductor substrate are formed in said interlayer insulating film by self-alignment in said high-density region with said first nitride film positioned on side of said gate electrodes as an etching stopper;

contact electrodes connected to said semiconductor substrate are formed from the contact holes formed in the interlayer insulating film; and

an interfacial level is recovered by annealing with a forming gas after each portion of said transistor elements is formed.

【Claim 4】

A method of manufacturing a circuit for forming a semiconductor device in which a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density exist on a single semiconductor substrate, is characterized in that;

a gate oxide film is formed on the surface of the high-density region and the low-density region of said semiconductor substrate;

gate electrodes of said transistor elements are formed in a predetermined high density arrangement at said high-density region, and in a predetermined low density arrangement at said low-density region, on the surface of the gate oxide film, after nitride protective films are separately formed on each surface;

a first nitride film having a predetermined thickness is uniformly formed on the surface of said high-density region and said low-density region;

said first nitride film is uniformly etched so that said nitride protective films are exposed at the surface of said gate electrodes and said gate oxide film is exposed in the gap;

the exposed gate oxide film is etched, therefore said semiconductor substrate is exposed in gaps between said gate electrodes of said high-density region and said low-density region;

a second nitride film having a predetermined thickness is formed on the surface of the exposed semiconductor substrate;

an interlayer insulating film with an impurity introduced therein is formed on the surface of said second nitride film;

a void which occurs in the interlayer insulating film disappears by annealing in an atmosphere containing water vapor;

contact holes reaching said semiconductor substrate are formed in said interlayer insulating film by self-alignment in said high-density region with said first nitride film positioned on side of said gate electrodes as an etching stopper;

contact electrodes connected to said semiconductor substrate are formed from the contact holes formed in the interlayer insulating film; and

an interfacial level is recovered by annealing with a forming gas after each portion of said transistor elements is formed.

【Claim 5】

A method of manufacturing a circuit according to any

one of claims 1-4, wherein said first nitride film and said second nitride film are formed by a CVD (chemical vapor deposition) process.

【Claim 6】

A method of manufacturing a circuit according to claim 3 or 4, wherein said first nitride film is formed by a CVD process, and said second nitride film is formed by a RTN (rapid thermal nitriding) process.

【Claim 7】

A method of manufacturing a circuit according to any one of claims 1-6,

wherein said first nitride film is formed to a thickness to serve as an etching stopper for said self-alignment, and

said second nitride film is formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into said semiconductor substrate by water-vapor annealing and also prevents said semiconductor substrate from being oxidized by water-vapor annealing, but allows said forming gas to be diffused into said semiconductor substrate.

【Claim 8】

A method of manufacturing a circuit according to claim 5, wherein said first nitride film is formed to a thickness of 30-50nm, and said second nitride film is formed to a thickness of 3.0-20nm.

【Claim 9】

A method of manufacturing a circuit according to claim 6, wherein said first nitride film is formed to a thickness of 30-50nm, and said second nitride film is formed to a thickness of 1.8-2.0nm.

【Claim 10】

A semiconductor device, in which a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density exist on a single semiconductor substrate, is characterized in that;

said semiconductor device is manufactured by a method of manufacturing a circuit according to any one of claims 1-9, and

said second nitride film is formed in at least a portion of the surface of the semiconductor substrate in said low-density region.

【Detailed Description of the Invention】

【0001】

【Field of the Invention】

The present invention relates to a method of manufacturing a circuit for forming a semiconductor device in which a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density exist on a single semiconductor substrate, and a

semiconductor device formed according to the method of manufacturing a circuit.

【0002】

【Prior Art】

There have heretofore been used semiconductor devices of various structures. For example, semiconductor memories such as DRAMs (Dynamic Random Access Memories) usually have a cell array region as a high-density region and a peripheral circuit region as a low-density region, disposed on a single semiconductor substrate.

【0003】

The cell array region comprises a two-dimensional high-density array of memory cells consisting of identical transistor elements, and the peripheral circuit region comprises a low-density array of various circuits such as an XY decoder. In manufacturing such a semiconductor device, the transistor elements in the high-density region and the transistor elements in the low-density region are simultaneously fabricated.

【0004】

One example of prior art of such a semiconductor device and a process of manufacturing the circuit will be described by way of example below with reference to FIGS. 18 through 20 of the accompanying drawings. FIG. 18 is a sectional front elevational view showing a multilayer structure of a DRAM as an example of prior art of

semiconductor device. FIG. 19 is a plan view of a cell array region as a high-density region of the DRAM. FIG. 20 is a sectional front elevational view of the DRAM in a fabrication process.

【0005】

As shown in FIG. 18, DRAM 100 which is shown as an example of prior art has a single semiconductor substrate 101. Cell array region 102 as a high-density region and peripheral circuit region 103 as a low-density region is made on the single semiconductor substrate 101.

【0006】

Cell array region 102 comprises a high-density array of identical transistor elements 111 that form memory cells 110, and peripheral circuit region 103 comprises a low-density array of transistor elements 112 that form various circuits including an XY decoder. Memory cells 110 consist of a pair of transistor elements 111 and a pair of capacitors 113 and are arranged in a substantially zigzag pattern and insulated each other by STI (Shallow Trench Isolation) 114 as shown in FIG. 19.

【0007】

Specifically, gate oxide films 115 are formed on the surface of semiconductor substrate 101 and gate electrodes 116 are formed on the surface of gate oxide films 115 in a pair of transistor elements 111 of memory cells 110. Gate electrode 116 comprises two layers including a polysilicon

layer 117 and a tungsten silicide layer 118. Oxide films 119 are formed on the surfaces of gate electrodes 116.

【0008】

Side walls 120 comprising nitride films are formed on sides of oxide films 119 and gate electrodes 116. Contact electrodes 121, 122 are formed in the gap between side walls 120 and on sides of side walls 120 of a pair of transistor elements 111 of memory cells 110.

【0009】

Contact electrodes 121 in the gap between a pair of transistor element 111 connect to source region (not shown) of semiconductor substrate 101 and to bit lines 123. A pair of contact electrodes 122 on the sides of a pair of transistor element 111 connects to a pair of drain region (not shown) of semiconductor substrate 101 and to a pair of capacitors 113.

【0010】

Transistor elements 112 of peripheral circuit region 103 are formed in the same construction as aforementioned transistor elements 111. Gate oxide films 115, gate electrodes 116 which consists of two layers 117, 118, and oxide layers 119 are laminated on the surface of semiconductor substrate 101. Side walls 120 consisting of nitride films are formed on sides of oxide films 119 and gate electrodes 116.

【0011】

In transistor elements 112 of peripheral circuit region 103, for example, aforementioned bit lines 123 are directly formed outside of side walls 120 and connected to drain regions 112 (not shown) of semiconductor substrate 101.

【0012】

A process of manufacturing circuit for forming DRAM 100 described above, will briefly be described below. STIs 114 are formed in a given pattern in cell array region 102 and peripheral circuit region 103 of semiconductor substrate 101. Then, gate oxide film 115 having a thickness of 8.0 (nm) is formed on the surface of semiconductor substrate 101 in an area free of STIs 114.

【0013】

Then, polysilicon layer 117 having a thickness of 100 (nm), tungsten silicide layer 118 having a thickness of 150 (nm), and oxide film 119 having a thickness of 150 (nm) are successively formed on the surface of gate oxide film 115, and thereafter etched in a given pattern to form gate electrodes 116 of transistor elements 111, 112.

【0014】

First nitride film 131 having a thickness of 50 (nm) is formed uniformly on the surface of cell array region 102 and peripheral circuit region 103 with gate electrodes 116 thus formed thereon. Cell array region 102 is masked, and first nitride film 131 in peripheral circuit region 103 is

etched to form side walls 120 on sides of gate electrodes 116 of peripheral circuit region 103 and expose gate oxide film 115 in the gap.

【0015】

After the mask is removed, oxide insulating film 132 having a thickness of 20 (nm) is uniformly formed on the surfaces of cell array region 102 and peripheral circuit region 103. As shown in FIG. 20, interlayer insulating film 133 made of BPSG (Borophosphosilicate Glass) with an impurity included and having a thickness of 1.0 (μm) is formed on the oxide insulating film 132.

【0016】

In cell array region 102, since gate electrodes 116 are arranged at a high density, voids 134 may possibly be formed in interlayer insulating film 133 as shown in figure. For this reason, interlayer insulating film 133 is annealed to reflow in an N_2 atmosphere, for example, to eliminate produced voids 134.

【0017】

Then, each portion is formed. For example, in cell array region 102, contact holes which reach semiconductor substrate 101 are formed in interlayer insulating film 133 by self-alignment using first nitride film 131 positioned on the sides of gate electrodes 116 as an etching stopper. Contact electrodes 121, 122 are then formed in the contact holes.

【0018】

After each portion of DRAM is formed, the assembly is annealed in a forming gas as of hydrogen to recover an interfacial level, finally. According to the above circuit fabrication process, it is possible to simultaneously form transistor elements 111 arranged at a high density in cell array region 102 and transistor elements 112 arranged at a low density in peripheral circuit region 103.

【0019】

In that case, since contact holes which reach semiconductor substrate 101 are formed in interlayer insulating film 133 by self-alignment using first nitride film 131 positioned on the sides of gate electrodes 116 as an etching stopper in cell array region 102, contact electrodes 121, 122 can reliably be formed in the gaps between transistor elements 111 that are arranged at a high density.

【0020】

If thick first nitride film 131 that can be used as an etching stopper has a large area, it generates excessive stresses when it is heated such as for annealing. Therefore, if it remains in the gaps between transistor elements 112 in peripheral circuit region 103, for example, drawbacks such as break of the crystalline structure of semiconductor substrate 101 are brought about. Because such thick first nitride film 131 blocks the forming gas

used in the final annealing step, if it remains in the gaps between transistor elements 112 in peripheral circuit region 103, then an interfacial level fails to be recovered.

【0021】

In the aforementioned circuit fabrication process, because thick first nitride film 131 as an etching stopper is removed in peripheral circuit region 103 where transistor elements 112 are arranged at a low density, the above various drawbacks is prevented beforehand.

【0022】

【Problems to Be Solved by the Invention】

In the aforementioned DRAM, since gate electrodes 116 are arranged at a high density in cell array region 102, voids 134 may possibly occur in interlayer insulating film 133. In that case, interlayer insulating film 133 is annealed to conduct reflowing to eliminate the voids 134.

【0023】

As a higher density is sought in semiconductor device such as the DRAM, the aspect ratio of interlayer insulating film 133 positioned in the gaps between gate electrodes 116 becomes larger. As shown in FIG. 21, if interlayer insulating film 133 positioned in the gaps between gate electrodes 116 has a width of 50 (nm) and a depth of 400 (nm), the aspect ratio thereof is 8. If the aspect ratio is 4 or higher, sufficient reflowing cannot be achieved in

interlayer insulating film 133 even if it is annealed, and voids 134 are liable to remain as shown in FIG. 22.

【0024】

In order to solve such problems, it is attempted to make the annealing temperature higher or to make the annealing time longer. However, an impurity such as phosphorus or boron was diffused from interlayer insulating film 133 into semiconductor substrate 101 in peripheral circuit region 103, making it impossible to control the characteristics of transistor elements 112.

【0025】

It is considerable to increase the thickness of oxide insulating film 132 to prevent it, but the aspect ratio of interlayer insulating film 133 positioned in the gaps between gate electrodes 116 is increased, making it more difficult to eliminate voids 134 in such case. It is also considerable increase the density of the impurity in interlayer insulating film 133 to allow easy reflowing of interlayer insulating film 133. However, the impurity diffusing from interlayer insulating film 133 into semiconductor substrate 101 in peripheral circuit region 103 is increased.

【0026】

The present inventor attempted to anneal interlayer insulating film 133 in an atmosphere containing water vapor, in order to conduct its reflowing well. By water-

vapor annealing, reflowing of interlayer insulating film 133 is conducted well without changing the annealing time and temperature. However, as shown in FIG. 23, it is proved that the impurity diffusing from interlayer insulating film 133 into semiconductor substrate 101 in peripheral circuit region 103 is also increased in such case.

【0027】

This appears to be due to the fact that the insufficient barrier capability of oxide insulating film 132 is impaired by the water-vapor annealing. It has been confirmed that silicon of semiconductor substrate 101 is oxidized in the water-vapor annealing. In this description, annealing in an atmosphere containing water vapor is referred as water-vapor annealing.

【0028】

The present invention is achieved under consideration the problems as mentioned above. Its object is to provide at least one of a method of manufacturing a circuit for forming a semiconductor device and a semiconductor device formed with that method, which has an array of transistor elements arranged at a high density, contact electrodes formed by self-alignment, and an interlayer insulating film free of voids.

【0029】

【Means to Solve the Problems】

In first method of manufacturing a circuit of this invention, a gate oxide film and gate electrodes are formed on a surface of a high-density region and a low-density region of a semiconductor substrate, then a first nitride film having a predetermined thickness is uniformly formed on those surface, then the first nitride film of the low-density region is etched while only the high-density region is masked, therefore the gate oxide film is exposed in gaps between the gate electrodes of the low-density region, then a second nitride film having a predetermined thickness is uniformly formed on the surface of the high-density region and the low-density region, then an interlayer insulating film with an impurity introduced therein is formed on a surface of the second nitride film, and then a void which occurs in the interlayer insulating film disappears by annealing in an atmosphere containing water vapor.

【0030】

Accordingly, in the method of manufacturing a circuit of this invention, voids in the interlayer insulating film are eliminated by water-vapor annealing. Since the gate oxide film and the second nitride film are positioned on the surface of the semiconductor substrate in the low-density region, the second nitride film prevents an impurity from being diffused from the interlayer insulating film into the semiconductor substrate and also prevents the semiconductor substrate from being oxidized. Generally, a

nitride film produces stresses when heated, e.g., when annealed, and cannot be formed in a large area in the low-density region. However, since the second nitride film has an appropriate thickness, it does not produce stresses that would impair the semiconductor substrate in the low-density region. Generally, a nitride film tends to prevent a forming gas used when the assembly is finally annealed from being diffused into the semiconductor substrate. However, since the second nitride film has an appropriate thickness, it does not prevent the forming gas from being diffused.

【0031】

In a second method of manufacturing a circuit of this invention, when a gate oxide film and gate electrodes are formed on a surface of a high-density region and a low-density region of a semiconductor substrate, nitride protective films are separately formed on each surface of the gate electrodes, then a first nitride film uniformly formed on the surface of the high-density region and the low-density region is uniformly etched so that the nitride protective films are exposed at the surface of the gate electrodes and the gate oxide film is exposed in the gap, then a second nitride film having a predetermined thickness is uniformly formed on the surface of the high-density region and the low-density region, then an interlayer insulating film with an impurity introduced therein is formed on a surface of the second nitride film, and then a

void which occurs in the interlayer insulating film disappears by annealing in an atmosphere containing water vapor.

【0032】

Accordingly, in the method of manufacturing a circuit of this invention, voids in the interlayer insulating film are eliminated by water-vapor annealing. Since the gate oxide film and the second nitride film are positioned on the surface of the semiconductor substrate in the low-density region, the second nitride film prevents an impurity from being diffused from the interlayer insulating film into the semiconductor substrate and also prevents the semiconductor substrate from being oxidized. Generally, a nitride film produces stresses when heated, e.g., when annealed, and cannot be formed in a large area in the low-density region. However, since the second nitride film has an appropriate thickness, it does not produce stresses that would impair the semiconductor substrate in the low-density region. Generally, a nitride film tends to prevent a forming gas used when the assembly is finally annealed from being diffused into the semiconductor substrate. However, since the second nitride film has an appropriate thickness, it does not prevent the forming gas from being diffused. When the first nitride film in the low-density region is removed, the first nitride film in the high-density region is also etched. However, since the nitride protective

films are formed on the gate electrodes, the gate electrodes are not exposed when the first nitride film in the high-density region is etched.

【0033】

In a third method of manufacturing a circuit of this invention, a gate oxide film and gate electrodes are formed on a surface of a high-density region and a low-density region of a semiconductor substrate, then a first nitride film having a predetermined thickness is uniformly formed on those surface, then the first nitride film of the low-density region is etched while only the high-density region is masked, therefore the gate oxide film is exposed in gaps between the gate electrodes of the low-density region, then the exposed gate oxide film is etched, therefore the semiconductor substrate is exposed in gaps between the gate electrodes of the low-density region, then a second nitride film having a predetermined thickness is formed on the surface of the exposed semiconductor substrate, then an interlayer insulating film with an impurity introduced therein is formed on a surface of the second nitride film, and then a void which occurs in the interlayer insulating film disappears by annealing in an atmosphere containing water vapor.

【0034】

Accordingly, in the method of manufacturing a circuit of this invention, voids in the interlayer insulating film

are eliminated by water-vapor annealing. Since the second nitride film is positioned on the surface of the semiconductor substrate in the low-density region, the second nitride film prevents an impurity from being diffused from the interlayer insulating film into the semiconductor substrate and also prevents the semiconductor substrate from being oxidized. Generally, a nitride film produces stresses when heated, e.g., when annealed, and cannot be formed in a large area in the low-density region. However, since the second nitride film has an appropriate thickness, it does not produce stresses that would impair the semiconductor substrate in the low-density region. Generally, a nitride film tends to prevent a forming gas used when the assembly is finally annealed from being diffused into the semiconductor substrate. However, since the second nitride film has an appropriate thickness, it does not prevent the forming gas from being diffused.

【0035】

In a fourth method of manufacturing a circuit of this invention, when a gate oxide film and gate electrodes are formed on a surface of a high-density region and a low-density region of a semiconductor substrate, nitride protective films are separately formed on each surface of the gate electrodes, then a first nitride film having a predetermined thickness is uniformly formed on a surface of a high-density region and a low-density region, then the

first nitride film is uniformly etched so that the nitride protective films are exposed at the surface of the gate electrodes and the gate oxide film is exposed in the gap, then the exposed gate oxide film is etched, therefore the semiconductor substrate is exposed in gaps between the gate electrodes of the high-density region and the low-density region, then a second nitride film having a predetermined thickness is formed on the surface of the exposed semiconductor substrate, then an interlayer insulating film with an impurity introduced therein is formed on a surface of the second nitride film, and then a void which occurs in the interlayer insulating film disappears by annealing in an atmosphere containing water vapor.

【0036】

Accordingly, in the method of manufacturing a circuit of this invention, voids in the interlayer insulating film are eliminated by water-vapor annealing. Since the second nitride film is positioned on the surface of the semiconductor substrate in the low-density region, the second nitride film prevents an impurity from being diffused from the interlayer insulating film into the semiconductor substrate and also prevents the semiconductor substrate from being oxidized. Generally, a nitride film produces stresses when heated, e.g., when annealed, and cannot be formed in a large area in the low-density region. However, since the second nitride film has an appropriate

thickness, it does not produce stresses that would impair the semiconductor substrate in the low-density region. Generally, a nitride film tends to prevent a forming gas used when the assembly is finally annealed from being diffused into the semiconductor substrate. However, since the second nitride film has an appropriate thickness, it does not prevent the forming gas from being diffused. When the first nitride film in the low-density region is removed, the first nitride film in the high-density region is also etched. However, since the nitride protective films are formed on the gate electrodes, the gate electrodes are not exposed when the first nitride film in the high-density region is etched.

[0037]

As another formation of this invention, the first nitride film and said second nitride film can be formed by a CVD process. In this case, the first nitride film and said second nitride film can be formed to respective desired thicknesses by the same process, so that the first nitride film is formed to a thickness to serve as an etching stopper for self-alignment and the second nitride film is formed to a thickness which prevents an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by water-vapor annealing and also prevents the semiconductor substrate from being oxidized by water-vapor annealing, but allows the forming gas to be

diffused into the semiconductor substrate.

【0038】

As another formation of this invention, the first nitride film can be formed by a CVD process, and the second nitride film can be formed by a RTN process. In this case, because the first nitride film can be formed to a desired thickness by the CVD process, the first nitride film is formed to a thickness to serve as an etching stopper for self-alignment. According to the RTN process, inasmuch as a nitride film cannot be formed on the surfaces of the oxide films, for example, after the oxide films on the surface of the semiconductor substrates on which the second nitride film is formed are removed, the exposed surface of the semiconductor substrate is heated in an ammonia atmosphere at a high temperature for a predetermined time to form the second nitride film. Since the RTN process can form a nitride film of good quality though the formed nitride film is thinner than a nitride film formed by the chemical vapor deposition process, the second nitride film is formed to prevent an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by water-vapor annealing and also prevent the semiconductor substrate from being oxidized by water-vapor annealing, but allows the forming gas to be diffused into the semiconductor substrate.

【0039】

As another formation of this invention, the first nitride film can be formed to a thickness to serve as an etching stopper for the self-alignment and the second nitride film can be formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into the semiconductor substrate by water-vapor annealing and also prevents said semiconductor substrate from being oxidized by water-vapor annealing, but allows said forming gas to be diffused into the semiconductor substrate.

【0040】

In this case, since the first and second nitride films have respective appropriate thicknesses, contact holes which reach the semiconductor substrate are formed in the interlayer insulating film by self-alignment in the high-density region. Further, an impurity of the interlayer insulating film is not diffused into the semiconductor substrate by water-vapor annealing and the semiconductor substrate is not oxidized by water-vapor annealing, but the forming gas is diffused into the semiconductor substrate.

【0041】

As another formation of this invention, the first nitride film can be formed to a thickness of 30-50nm, and the second nitride film can be formed to a thickness of 3.0-20nm. In this case, since the first and second nitride

films are formed to respective appropriate thicknesses by CVD process, the first and second nitride films are formed to have desired characteristics respectively.

【0042】

As another formation of this invention, the first nitride film can be formed to a thickness of 30-50nm, and the second nitride film can be formed to a thickness of 1.8-2.0nm. In this case, since the first nitride film is formed to an appropriate thickness by CVD process and the second nitride film having high quality is formed to an appropriate thickness by RTN process, the first and second nitride films are formed to have desired characteristics respectively.

【0043】

A semiconductor device of this invention, in which a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density exist on a single semiconductor substrate, is manufactured by the method of manufacturing a circuit according to this invention, and the second nitride film is formed in at least a portion of the surface of the semiconductor substrate in the low-density region.

【0044】

【Detailed Description of the Preferred Embodiments】

First embodiment of this invention will be described

below referring to FIGS. 1-9. Those parts which are identical to those of the prior art described above are referred to as identical nomenclature and denoted by identical reference numerals, and will briefly be described below.

【0045】

FIG. 1 is a sectional front elevational view showing an internal structure of a DRAM which is a first embodiment of a semiconductor device according to the present invention. FIGS. 2-6 are views showing fabrication stages of a first embodiment of a method of manufacturing a semiconductor device according to the present invention. FIG. 7 is a characteristics diagram showing rates at which an impurity is diffused from an interlayer insulating film into a semiconductor substrate via second nitride films having different thicknesses in a water-vapor atmosphere. FIG. 8 is a characteristics diagram showing oxidization resistance abilities when second nitride films having different thicknesses are water-vapor annealed. FIG. 9 is a characteristics diagram showing the relationship between thicknesses of second nitride films and rates at which an interfacial level is recovered by annealing in a forming gas.

【0046】

As shown in FIG. 8, in DRAM 200 as the first embodiment of a semiconductor device according to this

invention, cell array region 102 as a high-density region and peripheral circuit region 103 as a low-density region is disposed on single semiconductor substrate 101, similar to DRAM 100 as a prior art.

【0047】

In cell array region 102, transistor elements 111 that form memory cells 110 are disposed in a predetermined high-density array, and in peripheral circuit region 103, transistor elements 112 that form various circuits including an XY decoder are disposed in a predetermined low-density array. Memory cells 110 comprising a pair of transistor elements 111 and a pair of capacitors 113 is isolated each other by STI 114 and arranged in a two-dimensional zigzag pattern.

【0048】

Specifically, in a pair of transistor elements 111 of memory cells 110, gate oxide films 115 are formed on the surface of semiconductor substrate 101 and gate electrodes 116 are formed on a surface of the gate oxide films 115. The gate electrodes 116 are formed in two-layer structure including polysilicon layer 117 and tungsten silicide layer 118, and oxide films 119 are formed on those surface.

【0049】

Side walls 120 consisting of nitride films are formed on sides of the oxide films 119 and gate electrodes 116. Contact electrodes 121,122 are formed in the gaps between

side walls 120 and on sides of side walls 120 of a pair of transistor elements 111 of memory cells 110.

【0050】

Contact electrode 121 in the gap between a pair of transistor elements 111 is connected to source region (not shown) of semiconductor substrate 101 and bit line 123. Pair of contact electrodes 122 on the both sides of a pair of transistor elements 111 are connected to a pair of drain region (not shown) of semiconductor substrate 101 and a pair of capacitor 113, respectively.

【0051】

Transistor elements 112 in peripheral circuit region 103 is formed in the same structure as the transistor elements 111 described above. Gate oxide films 115, two layers 117,118 forming gate electrodes 116, and oxide films 119 are formed on the surface of semiconductor substrate 101. Side walls 120 consisting of nitride films are formed on sides of the oxide films 119 and gate electrodes 116.

【0052】

In transistor elements 112 in peripheral circuit region 103, the above described bit line 123 is directly formed on the outside of the side wall 120 and connected to a drain region (not shown) of semiconductor substrate 101

【0053】

A method of manufacturing the above DRAM 100 will be consecutively described below. Firstly, as shown in FIG.

2(a), STIs 114 are formed in a given pattern in cell array region 102 and peripheral circuit region 103 of semiconductor substrate 101. Gate oxide film 115 having a thickness of 8.0 nm is formed on the surface of semiconductor substrate 101 in an area free of STIs 114.

【0054】

Then, polysilicon layer 117 having a thickness of 100 nm, tungsten silicide layer 118 having a thickness of 150 nm, and oxide film 119 having a thickness of 150 nm are successively formed on the surface of gate oxide film 115. As shown in FIG. 2(b), they are etched in predetermined pattern to form gate electrodes 116.

【0055】

In this way, first nitride film 131 having a thickness of 40 nm is uniformly formed by CVD process on the surface of cell array region 102 and peripheral circuit region 103 where the gate electrodes 116 are formed. As shown in FIG. 3(a), only cell array region 102 is masked by a resist 201, and first nitride film 131 in peripheral circuit region 103 is etched so as to form side walls 120 on sides of gate electrodes 116 in peripheral circuit region 103 and to expose gate oxide film 115 in the gaps.

【0056】

Then, as shown in FIG. 3(b), after resist 201 is removed, second nitride film 202 having a thickness of 10 nm is uniformly formed on the surfaces of cell array region

102 and peripheral circuit region 103. As shown in FIG. 4(a), interlayer insulating film 133 made of BPSG with an impurity included and having a thickness of 1.0 μm is formed on the surface of second nitride film 202.

【0057】

In this embodiment, gate electrodes 116 are arranged at a high density in cell array region 102 and voids 134 are formed in interlayer insulating film 133. For this reason, interlayer insulating film 133 is annealed for 10 minutes to conduct reflowing in an atmosphere containing water vapor at 800 ℃ to eliminate produced voids 134, as shown in FIG. 4(b).

【0058】

Then, as shown in FIG. 5(a), the surface of interlayer insulating film 133 is planarized by a CMP (Chemical Mechanical Polishing) process and oxide film 203 is formed on that surface. The surface of oxide film 203 is masked in a given pattern by a KrF resist and contact holes 204 are formed on both sides of gate electrodes 116 at the position of the transistor element 111 in cell array region 102 as shown in FIG. 6(a).

【0059】

At this time, since first nitride film 131 having a thickness of 40 nm is positioned on the surface and sides of gate electrodes 116 as shown in FIG. 5(b), contact holes 204 which reach semiconductor substrate 101 are formed in

interlayer insulating film 133 by self-alignment using it as an etching stopper as shown in FIG. 6(a).

【0060】

Then, as shown in FIG. 6(b), contact electrodes 121, 122 are formed in the contact holes 204 by etchback. After that, each portion of DRAM 200 is formed in the same way as prior art. Finally, the assembly is annealing in a forming gas as of hydrogen is conducted to recover an interfacial level.

【0061】

In the above described construction, DRAM 200 of the present embodiment is constructed like DRAM 100 of prior art. However, second nitride film 202 having a thickness of 10 nm is formed on the surface where the gate electrodes 116 and bit line 123 are not positioned in peripheral circuit region 103 of semiconductor substrate 101, instead of the oxide film 132.

【0062】

In the method of manufacturing a circuit of this invention, similar to prior art, it is possible to simultaneously form transistor elements 111 arranged at a high density in cell array region 102 and transistor elements 112 arranged at a low density in peripheral circuit region 103, and to reliably form contact electrodes 121, 122 in the gaps between transistor elements 111 arranged at a high density because contact holes 204 which

reach semiconductor substrate 101 are formed in interlayer insulating film 133 by self-alignment using first nitride film 131 on sides of gate electrodes 116 as an etching stopper in cell array region 102.

【0063】

However, in the method of manufacturing a circuit according to the present embodiment, differing from prior art, because interlayer insulating film 133 is water-vapor annealed to conduct reflowing, voids 134 which occur in it can well be eliminated. Further, since second nitride film 202 having a thickness of 10 nm is interposed between interlayer insulating film 133 and semiconductor substrate 101 in peripheral circuit region 103, the impurity in interlayer insulating film 133 is prevented from being diffused into semiconductor substrate 101 by water-vapor annealing and silicon of semiconductor substrate 101 is prevented from being oxidized by the water-vapor annealing.

【0064】

As described above, if first nitride film 131 having a thickness of 40 nm which serves as an etching stopper has a large area, it generate excessive stresses to bring about a drawback such as break of the crystalline structure of semiconductor substrate 101 when it is heated such as for annealing. However, second nitride film 202 having a thickness of 10 nm does not generate stresses large enough to break the crystalline structure of semiconductor

substrate 101. Further, the second nitride film having a thickness of 10 nm well passes the forming gas used in the final annealing step, it does not impair the recovery of an interfacial level.

【0065】

The present inventor actually conducted various tests to verify the performance of DRAM 200 manufactured by the above method of manufacturing a circuit. Firstly, samples, in which interlayer insulating film 133 is laminated on the surface of semiconductor substrate 101 with second nitride film 202 of various thickness interposed therebetween, were produced and water-vapor annealed in for 10 minutes at 800 ℃.

【0066】

As a result, as shown in FIG. 7, it was confirmed that if the thickness of second nitride film 202 was 2.0 nm or more, the diffusion of an impurity from interlayer insulating film 133 into semiconductor substrate 101 was prevented substantially completely, and if its thickness was 4.0 nm or more, the diffusion of an impurity was prevented steadily. Further, it was confirmed that when water-vapor annealing was conducted in for 30 minutes at 850 ℃, if the thickness of second nitride film 202 was 3.0 nm or more, the diffusion of an impurity was prevented substantially completely, and if its thickness was 5.0 nm or more, the diffusion of an impurity was prevented

steadily (not shown).

【0067】

Samples having second nitride films 202 formed on the surface of semiconductor substrate 101 were water-vapor annealed for 10 minutes at 800 ℃, and the rate of oxidization of semiconductor substrate 101 was tested according to change of the thickness of second nitride films 202. As a result, as shown in FIG. 8, it was confirmed that if the thickness of second nitride film 202 was 3.0 nm or more, semiconductor substrate 101 was prevented substantially completely from being oxidized by the water-vapor annealing, and if the thickness was 5.0 nm or more, semiconductor substrate 101 was prevented steadily from being oxidized.

【0068】

Further, DRAMs 200 were trial produced and annealed at 400 ℃ using a forming gas of hydrogen. As a result, as shown in FIG. 9, It was confirmed that if the thickness of second nitride film 202 was 20 nm, the forming gas was not diffused into semiconductor substrate 101 and an interfacial level of various parts was not recovered, but if the thickness was 10 nm or less, the forming gas was well diffused into semiconductor substrate 101, an interfacial level of various parts was well recovered.

【0069】

It was also confirmed that when the annealing was

conducted under various conditions, if the thickness of second nitride film 202 was 30 nm or less, semiconductor substrate 101 suffered no stress-dependent faults (not shown).

【0070】

In the method of manufacturing DRAM 200 according to the present embodiment, first nitride film 131 is formed by CVD process to a thickness in a range from 30 to 50 nm, to serve an etching stopper for self-alignment. However, Second nitride film 202 is formed by CVD process to a thickness in a range from 3.0 to 20 nm, more preferably in a range from 5.0 to 15 nm, to prevent the impurity of interlayer insulating film 133 from being diffused into semiconductor substrate 101 by the water-vapor annealing and also prevent semiconductor substrate 101 from being oxidized by the water-vapor annealing, but allow the forming gas to be diffused into semiconductor substrate 101.

【0071】

A second embodiment of this invention will be described below with reference to FIGS. 10-13. Those parts which are identical to those of the first embodiment described above are referred to as identical nomenclature and denoted by identical reference numerals, and will briefly be described.

【0072】

FIG. 10 is a sectional front elevational view showing an internal structure of a DRAM which is second embodiment of a semiconductor device according to the present invention. FIGS. 11-13 are views showing fabrication stages of second embodiment of the method of manufacturing a circuit according to the present invention.

【0073】

DRAM 300 as a second embodiment of a semiconductor device of the present invention has the substantially same structure as that of DRAM 200 according to the first embodiment. However, unlike DRAM 200 of the first embodiment, nitride protective film 301 is formed on the surface of each gate electrode 116 instead of oxide film 119, and no first nitride film 131 remains on the surface of each gate electrode 116 as shown in FIG. 17.

【0074】

A method of manufacturing aforementioned DRAM 300 will briefly be described below. Firstly, gate oxide films 115 are formed on the surface of semiconductor substrate 101, then polysilicon layers 117, tungsten silicide layers 118, and nitride protective film 301 having a thickness of 150 nm is formed successively, and then they are etched in a given pattern to form gate electrodes 116 of transistor elements 111,112.

【0075】

As shown in FIG. 11(a), first nitride film 131 having

a thickness of 40 nm is uniformly formed on the surface of each region 102,103 by CVD process and the uniformly etched to form side wall 120 on sides of gate electrodes 116 of each region 102,103 and to expose gate oxide films 115 in the gaps, as shown in FIG. 11(b).

【0076】

At this time, since nitride protective film 301 is formed on the surface of gate electrodes 116 instead of oxide film 119, if first nitride film 131 is etched until gate oxide films 115 is exposed, nitride protective film 301 on the surface of gate electrodes 116 is exposed.

【0077】

After that, in the same way as first embodiment, second nitride film 202 having a thickness of 10 nm is uniformly formed on the surfaces of each region 102,103 as shown in FIG. 12(a), and interlayer insulating film 133 made of BPSG with an impurity included and having a thickness of 1.0 μm is formed on the surface of second nitride film 202 as shown in FIG. 12(b).

【0078】

As shown in FIG. 13(a), interlayer insulating film 133 is water-vapor annealed at 800 ℃ for 10 minutes to conduct reflowing to eliminate voids 134. As shown in FIG. 13(b), oxide film 203 is formed on the planarized surface of interlayer insulating film 133, and contact electrodes 121,122 are formed on both sides of gate electrodes 116 at

the position of the transistor element 111 in cell array region 102.

【0079】

When contact holes 204 buried by contact electrodes 121,122 are formed by self-alignment, side walls 120 consisting of first nitride film 301 exist on sides of gate electrodes 116, first nitride film 131 on the surface of gate electrodes 116 is etched.

【0080】

However, since nitride protective film 301 having a thickness of 150 nm is positioned on the surface of gate electrodes 116 where first nitride film 131 is etched, contact holes 204 which reach semiconductor substrate device are formed in interlayer insulating film 133 by self-alignment using nitride protective film 301 and sidewalls 120 as etching stoppers.

【0081】

In the above described construction, DRAM 300 of the second embodiment is constructed like DRAM 200 of the first embodiment. However, nitride protective film 301 is formed on each surface of the gate electrodes 116 instead of oxide film 119. Since nitride protective film 301 serves as an etching stopper on the surface of gate electrodes 116 when contact holes 204 are formed by self-alignment, it is unnecessary to leave first nitride film 131 on the surface of gate electrodes 116.

【0082】

With DRAM 300 according to the present embodiment, when first nitride film 131 is removed from the surface of peripheral circuit region 103, cell array region 102 does not need to be masked, and first nitride film 131 can be uniformly etched in each regions 102, 103. Therefore it can be manufactured easily with good productivity.

【0083】

The present invention is not limited to the above embodiments and variations will be allowed without departing from the scope. For example, it is explained with an example that both first and second nitride films 131, 202 do not need to be formed by CVD process in the above embodiment, but only first nitride film 131 may be formed by CVD process and second nitride film may be formed by an RTN process.

【0084】

Since a nitride film formed by the RTN process has good quality though it is thinner than a nitride film formed by CVD process, it is possible to form second nitride film 400 having a thickness in a range from 1.8 to 2.0 nm and sufficient characteristics. However, according to the RTN process, it is impossible to grow a nitride film on the surface of an oxide film.

【0085】

Therefore, for forming second nitride film 400 of

DRAM 200 according to the said first embodiment by the RTN process, it is preferable to mask only cell array region 102, remove gate oxide films 115 with fluorine in peripheral circuit region 103 as shown in FIG. 3(a), and heat the exposed surface of semiconductor substrate 101 in an ammonia atmosphere at about 850 ℃ for 60 seconds according to the RTN process to form second nitride film 400, as shown in FIG. 14.

【0086】

For forming second nitride film 400 of DRAM 300 according to the second embodiment by the RTN process, it is preferable to etch first nitride film 131 in regions 102, 103 to expose gate oxide films 115, remove exposed gate oxide films 115 with fluorine, as shown in FIG. 18B, and form second nitride film 400 on the exposed surface of semiconductor substrate 101 according to the RTN process, as shown in FIG. 21.

【0087】

Furthermore, after removing gate oxide films 115 of DRAMs 200, 300 with fluorine to expose semiconductor substrate 101 as described above, second nitride film 401 having a desired thickness can be formed by CVD process, as shown in FIGS. 16 and 17.

【0088】

【Effect of the Invention】

In the method of manufacturing a circuit of this

invention, by forming second nitride film on the surface in the low-density region of the semiconductor substrate, even voids in the interlayer insulating film are eliminated by water-vapor annealing, an impurity can be prevented from being diffused from the interlayer insulating film into the semiconductor substrate by the second nitride film, and if the second nitride film has an appropriate thickness, the semiconductor substrate is not damaged in the low-density region by excessive stresses in annealing, and it is prevented to impair diffusion of the forming gas and recovery of interfacial level of various parts of semiconductor circuit.

【0089】

In the second and fourth method of manufacturing a circuit of this invention, by forming nitride protective film on the surface of gate electrodes, when first nitride film 131 is uniformly etched in the low-density region and the high-density region, gate electrodes are not exposed, and it is unnecessary to mask the high-density region when first nitride film 131 is removed in the low-density region, therefore productivity can be improved.

【0090】

By forming first nitride film and second nitride film with the CVD process, since the first nitride film and said second nitride film can be formed to respective desired thicknesses by the same process, so that the first nitride

film can be formed to a thickness to serve as an etching stopper for self-alignment and the second nitride film can be formed to a thickness which prevents an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by water-vapor annealing and also prevents the semiconductor substrate from being oxidized by water-vapor annealing, but allows the forming gas to be diffused into the semiconductor substrate.

【0091】

By forming first nitride film with the CVD process and forming second nitride film with the RTN process, the first nitride film can be formed to a thickness to serve as an etching stopper for self-alignment, and since a nitride film can be formed with the RTN process in good quality though it is thinner than a nitride film formed by CVD process, the second nitride film can be formed to prevent an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by water-vapor annealing and also to prevent the semiconductor substrate from being oxidized by water-vapor annealing, but to allow the forming gas to be diffused into the semiconductor substrate.

【0092】

By forming first nitride film and second nitride film to respective desired thicknesses in this way, contact holes which reach the semiconductor substrate can be formed

in the interlayer insulating film by self-alignment in the high-density region, an impurity of the interlayer insulating film can be prevented from being diffused into the semiconductor substrate by water-vapor annealing, and the semiconductor substrate can be prevented from being oxidized by water-vapor annealing, and the forming gas can be diffused into the semiconductor substrate, therefore it is possible to manufacture the high-performance semiconductor device.

【Brief Description of the Drawings】

【FIG.1】

It is a sectional front elevational view showing an internal structure of a DRAM as first embodiment of a semiconductor device according to the present invention.

【FIG.2】

It is a part of views showing fabrication stages of the first embodiment of the method of manufacturing a circuit according to the present invention.

【FIG.3】

It is a part of the above views showing fabrication.

【FIG.4】

It is a part of the above views showing fabrication.

【FIG.5】

It is a part of the above views showing fabrication.

【FIG.6】

It is a part of the above views showing fabrication.

【FIG.7】

It is a characteristics diagram showing rates at which an impurity is diffused from an interlayer insulating film into a semiconductor substrate via second nitride films having various thicknesses by water-vapor annealing.

【FIG.8】

It is a characteristics diagram showing oxidization resistance abilities when second nitride films having various thicknesses are water-vapor annealed.

【FIG.9】

It is a characteristics diagram showing the relationship between thicknesses of second nitride films and rates at which an interfacial level is recovered by annealing in a forming gas.

【FIG.10】

It is a sectional front elevational view showing an internal structure of a DRAM as second embodiment of a semiconductor device according to the present invention.

【FIG.11】

It is a part of view showing fabrication stages of the second embodiment of the method of manufacturing a circuit according to the present invention.

【FIG.12】

It is a part of the above views showing fabrication.

【FIG.13】

It is a part of the above views showing fabrication.

【FIG.14】

It is a sectional front elevational view showing a fabrication stage of first modification of DRAM of the first embodiment.

【FIG.15】

It is a sectional front elevational view showing a fabrication stage of first modification of DRAM of the second embodiment.

【FIG.16】

It is a sectional front elevational view showing a fabrication stage of second modification of DRAM of the first embodiment.

【FIG.17】

It is a sectional front elevational view showing a fabrication stage of second modification of DRAM of the second embodiment.

【FIG.18】

It is a sectional front elevational view showing a multilayer structure of a DRAM as one example of prior art semiconductor device.

【FIG.19】

It is a schematic plan view of a cell array region as a high-density region of the DRAM.

【FIG.20】

It is a schematic sectional front elevational view showing DRAM in fabrication.

【FIG.21】

It is a schematic sectional front elevational view showing size of each portion of DRAM in fabrication.

【FIG.22】

It is a schematic sectional front elevational view showing a defect as voids remaining in the DRAM in fabrication

【FIG.23】

It is a characteristics diagram showing rates at which an impurity is diffused from an interlayer insulating film via an oxide film into a semiconductor substrate in annealing in a nitrogen atmosphere and a water-vapor atmosphere.

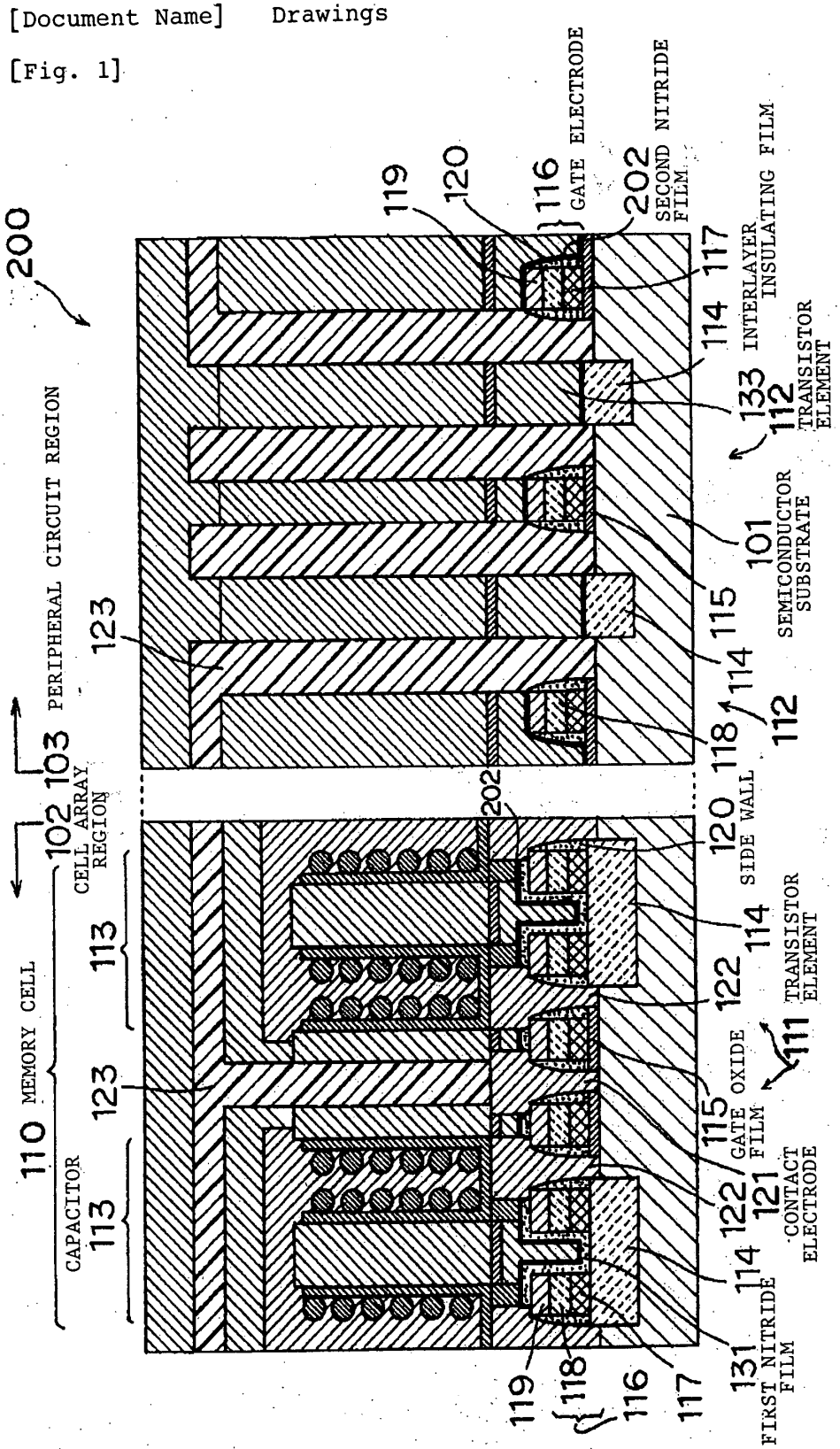
【Description of Numbers】

101	semiconductor substrate
102	cell array region as a high-density region
103	peripheral circuit region as a low-density region
111,112	transistor element
115	gate oxide film
116	gate electrode
121,122	contact electrode
131	first nitride film
134	void
200,300	DRAM as a semiconductor device
202,400,401	second nitride film
204	contact hole

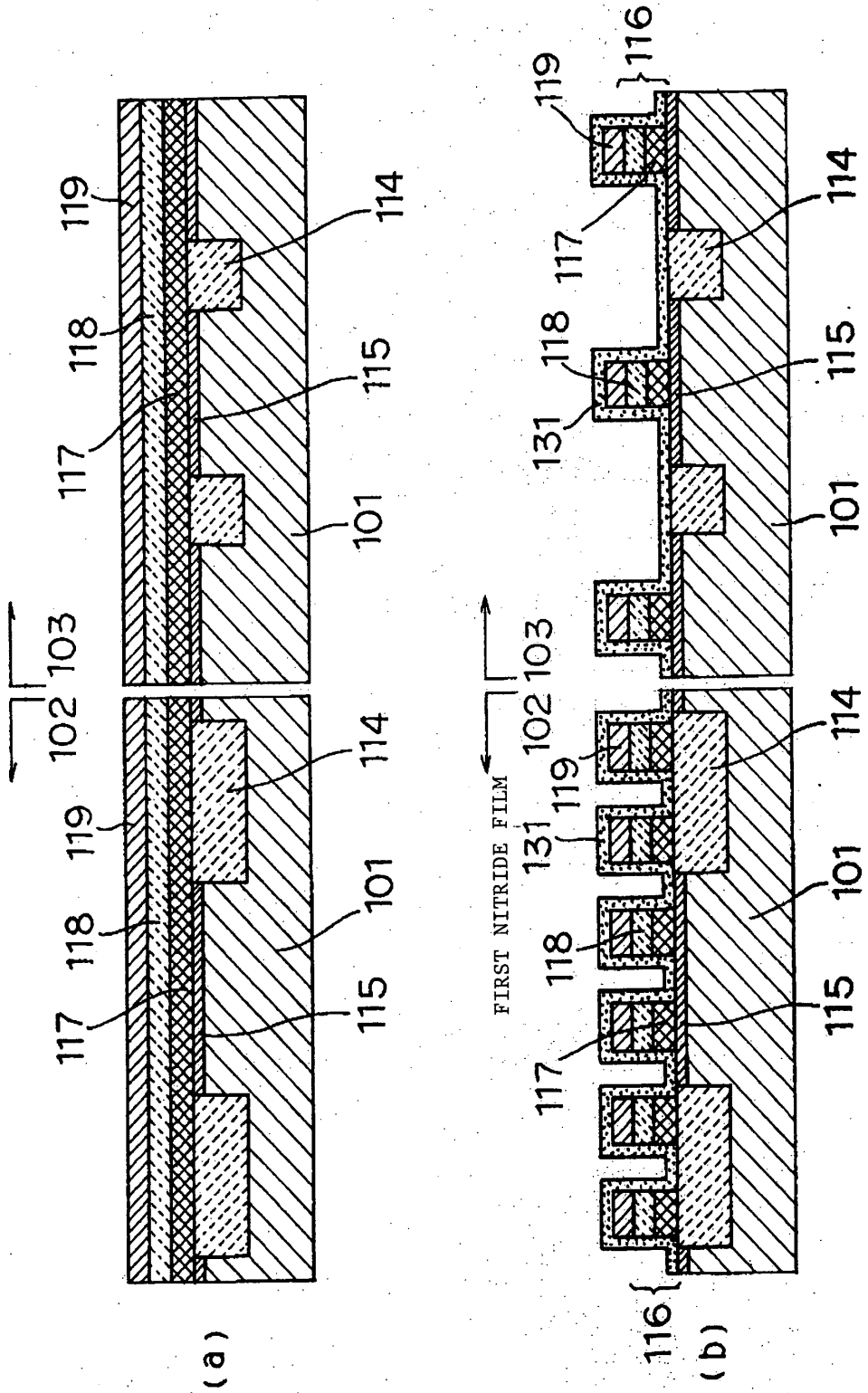
301 nitride protective film

[Document Name] Drawings

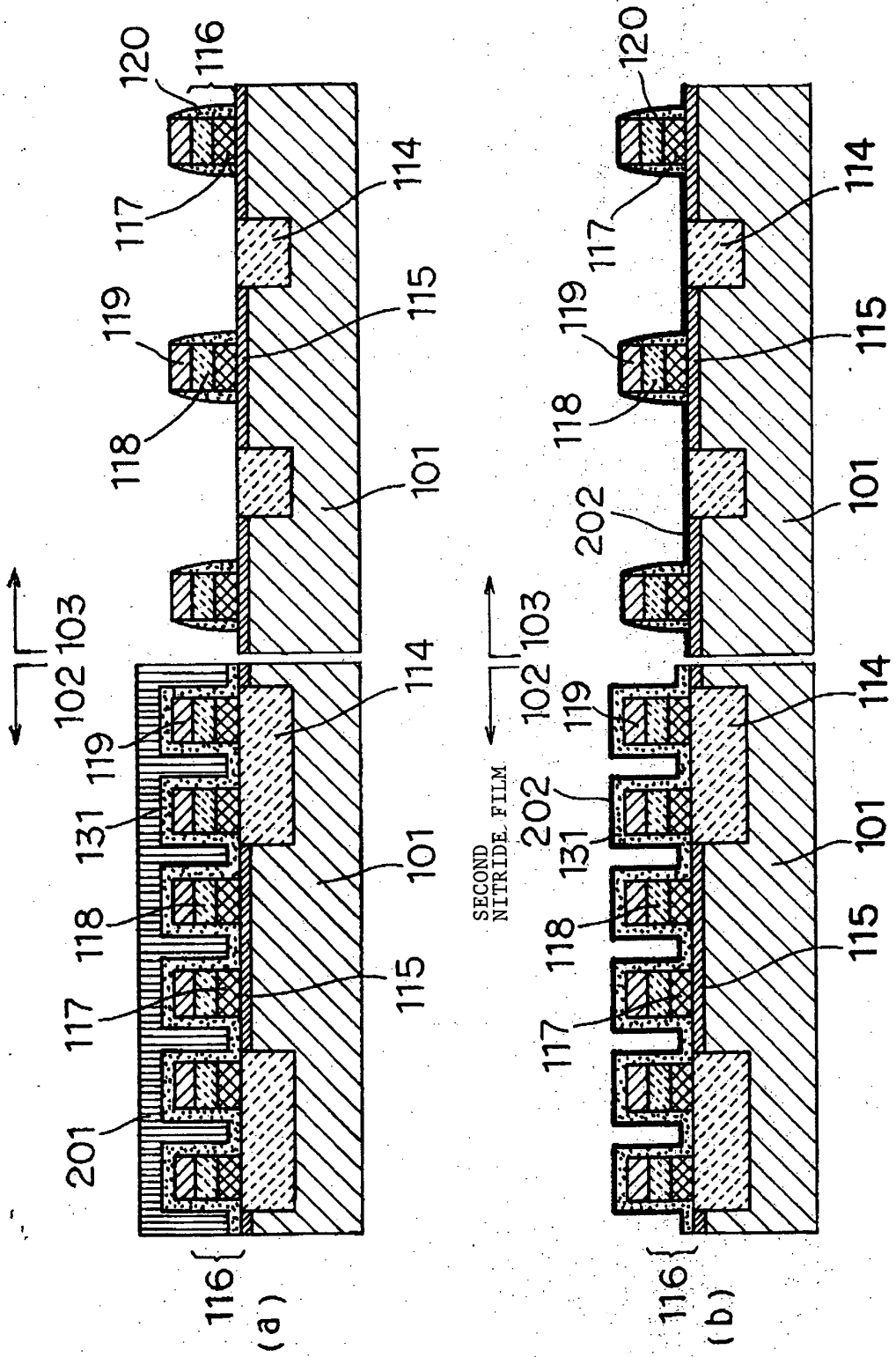
[Fig. 1]



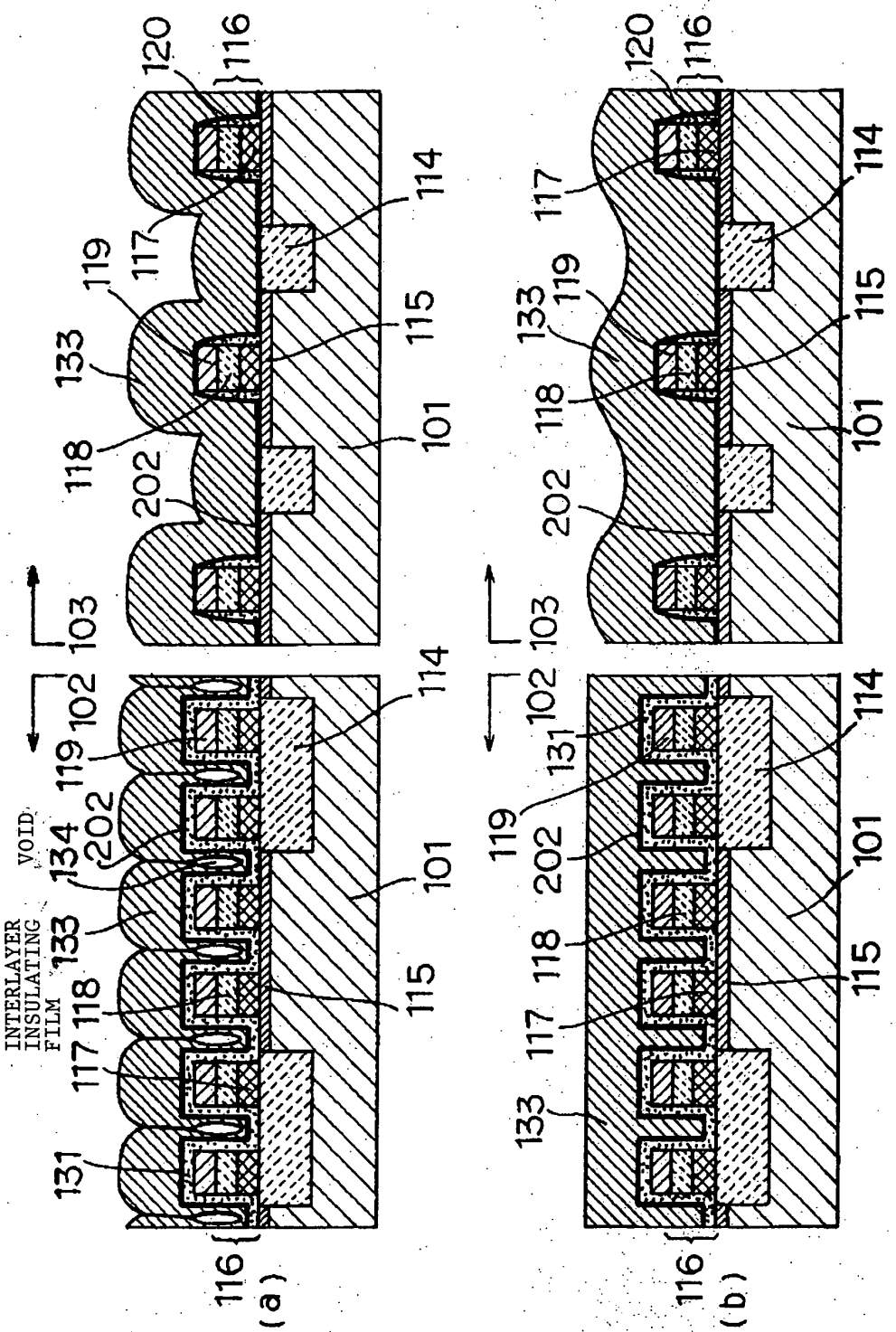
[Fig. 2]



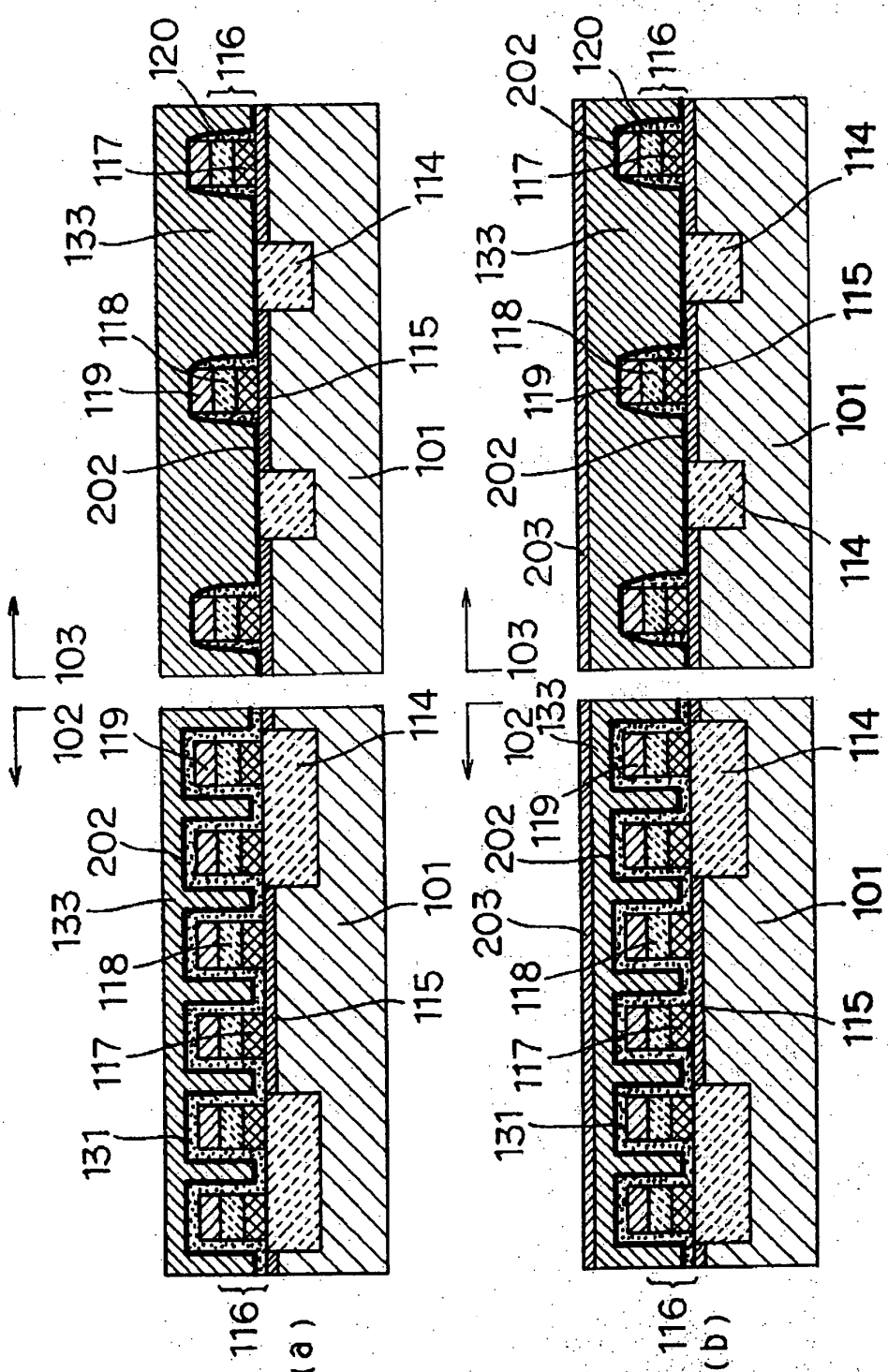
[Fig. 3]


120
116
117
114
119
115
118
101
102
103
131
201
(a)
SECOND NITRIDE FILM
202
(b)

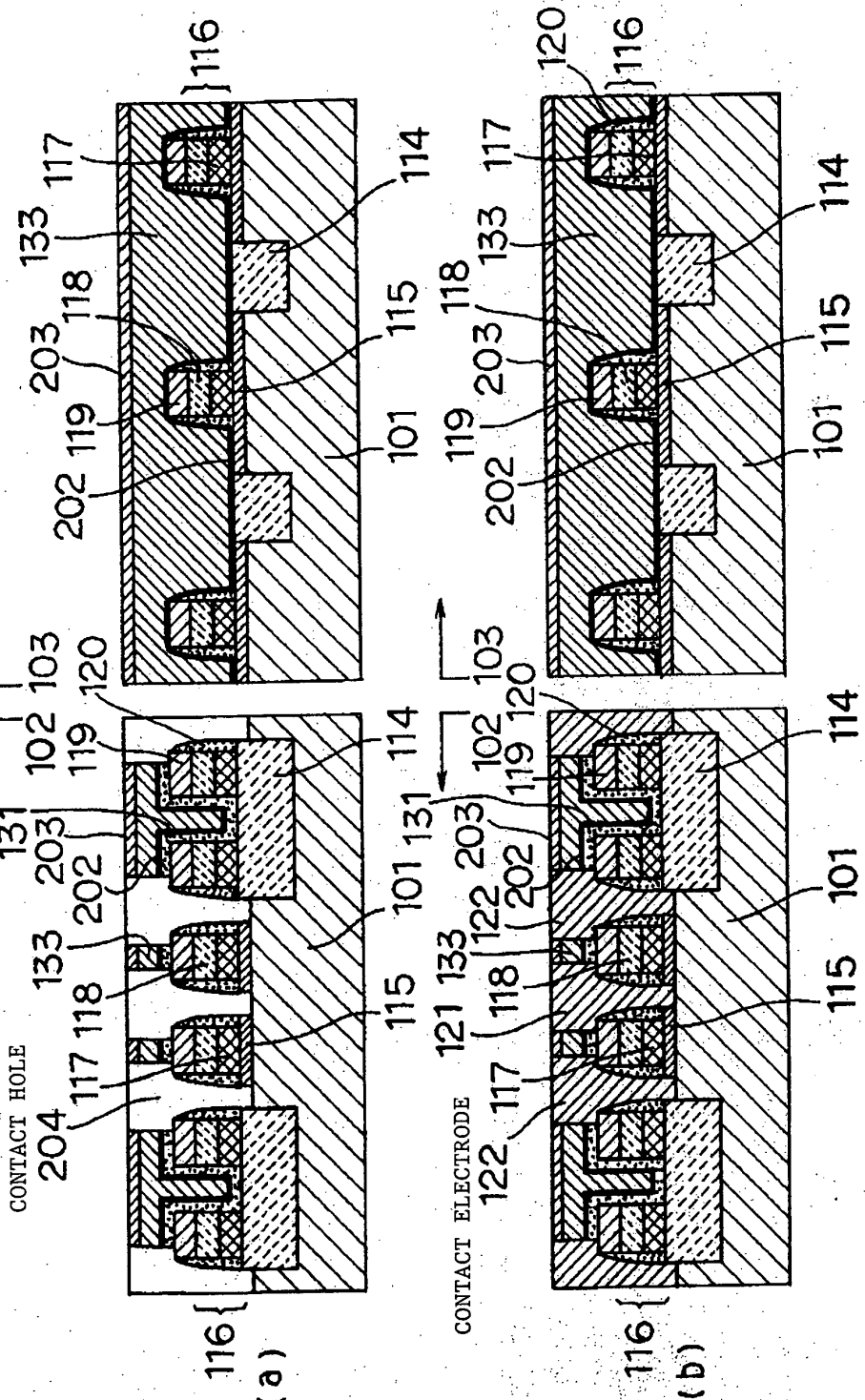
[Fig. 4]


120
116
114
119
117
133
115
118
101
202
103
102
131
VOID
134
INTERLAYER INSULATING FILM
(a)
(b)

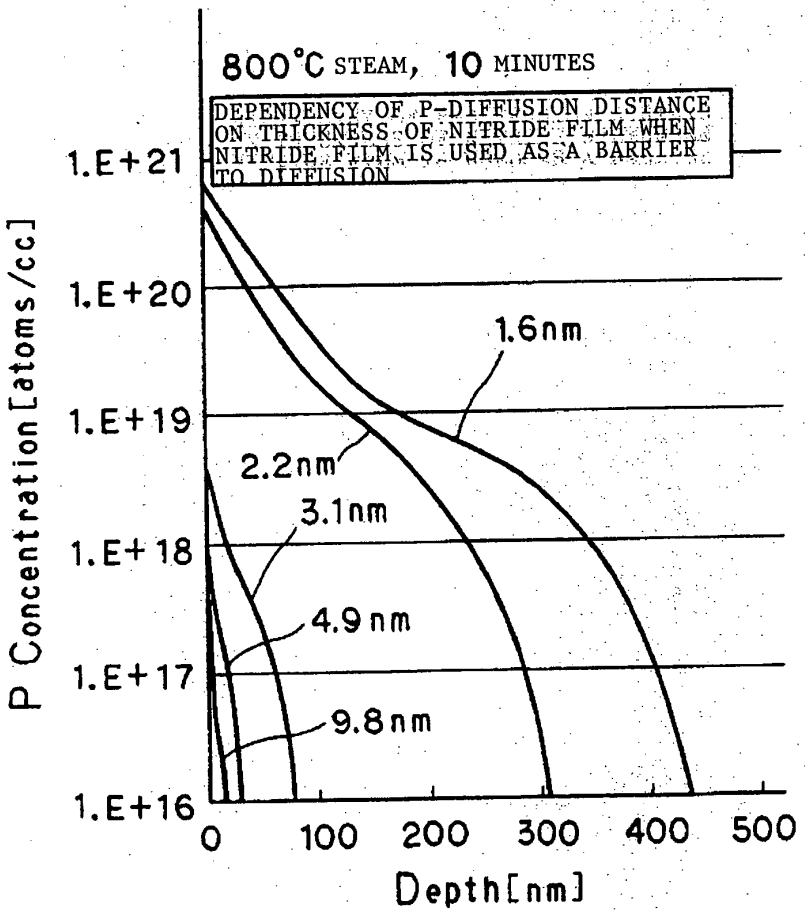
[Fig. 5]



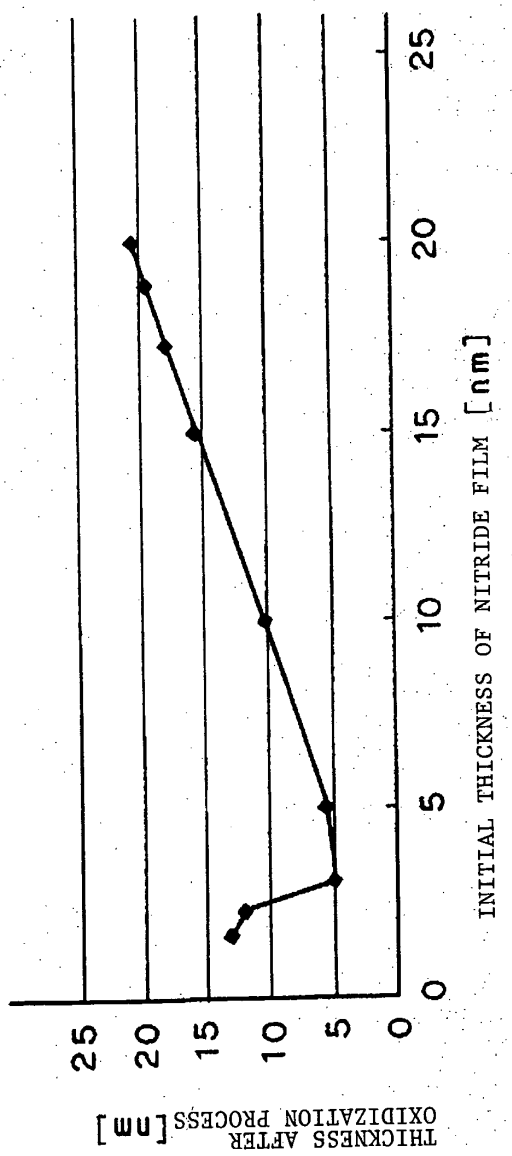
[Fig. 6]



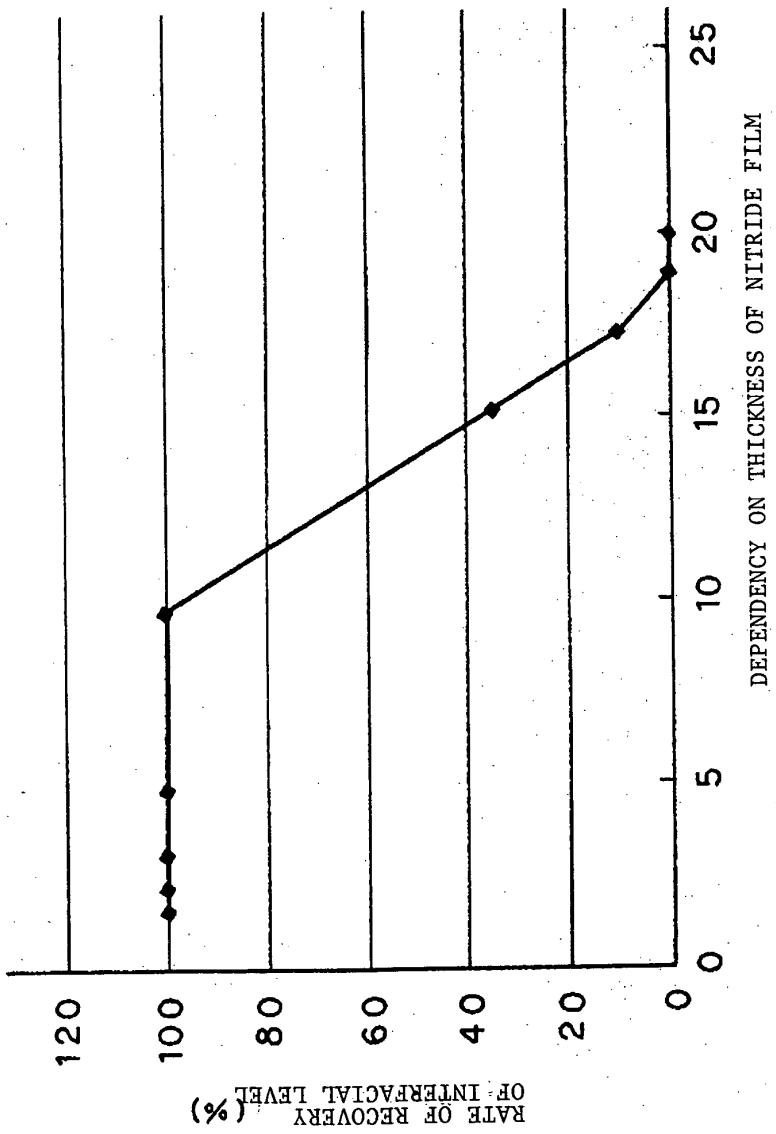
[Fig. 7]


800°C STEAM, 10 MINUTES
DEPENDENCY OF P-DIFFUSION DISTANCE ON THICKNESS OF NITRIDE FILM WHEN NITRIDE FILM IS USED AS A BARRIER TO DIFFUSION
1.E+21
1.E+20
1.E+19
1.E+18
1.E+17
1.E+16
P Concentration [atoms/cc]
1.6nm
2.2nm
3.1nm
4.9nm
9.8nm
0
100
200
300
400
500
Depth [nm]

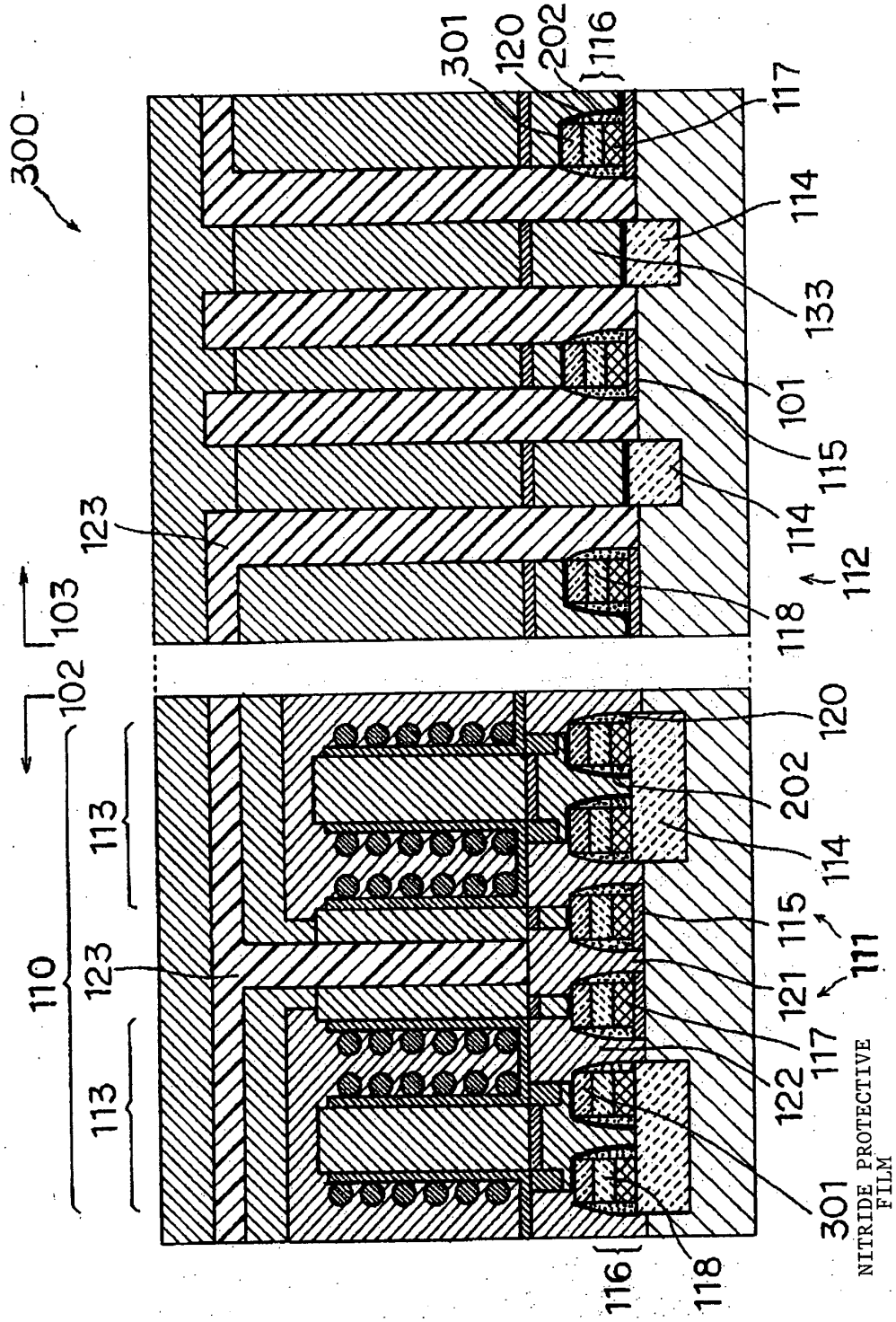
[Fig. 8]


THICKNESS AFTER OXIDIZATION PROCESS [nm]
25
20
15
10
5
0
0
5
10
15
20
25
INITIAL THICKNESS OF NITRIDE FILM [nm]

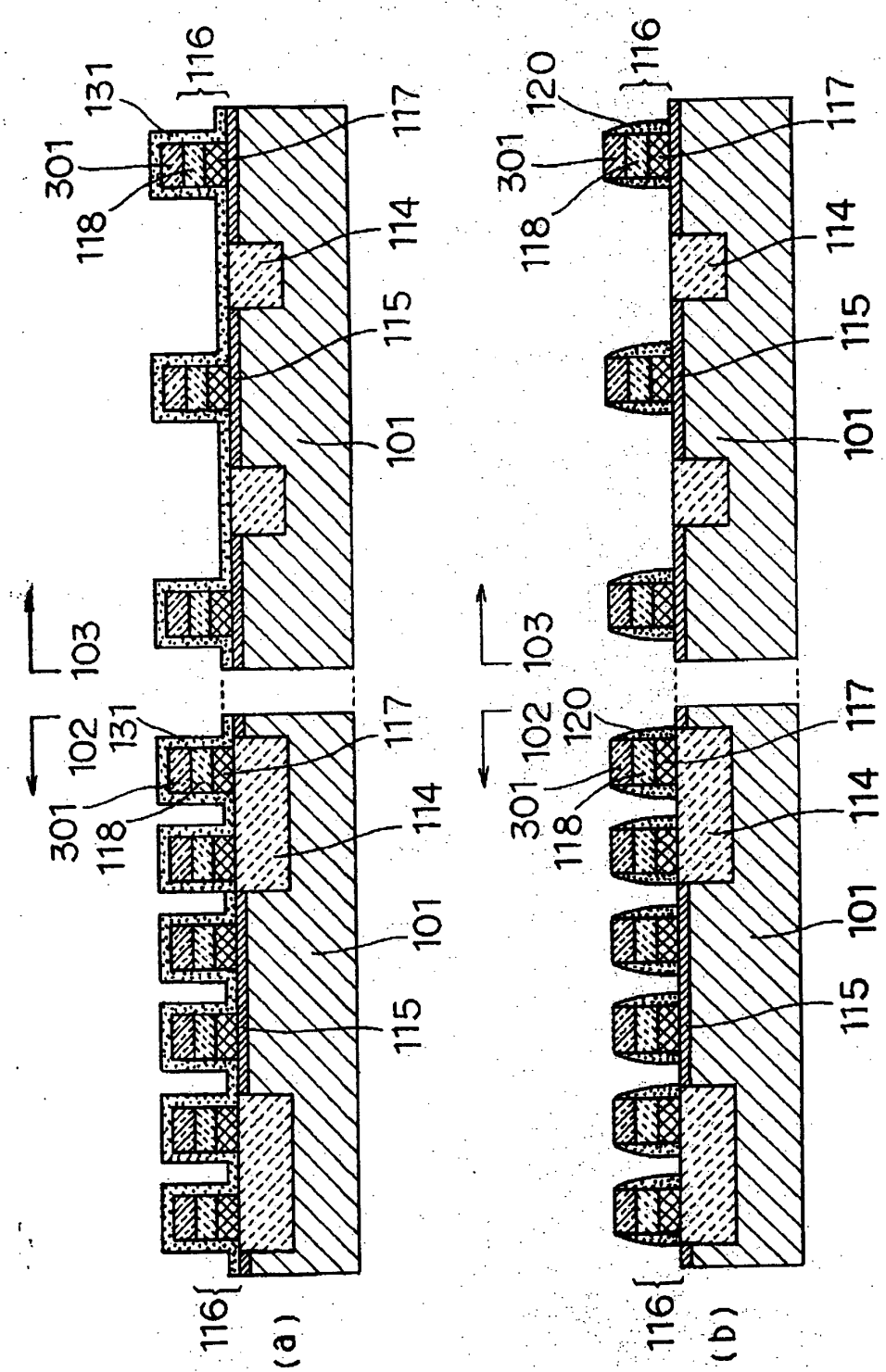
[Fig. 9]


RATE OF RECOVERY OF INTERFACIAL LEVEL (%)
120
100
80
60
40
20
0
0
5
10
15
20
25
DEPENDENCY ON THICKNESS OF NITRIDE FILM

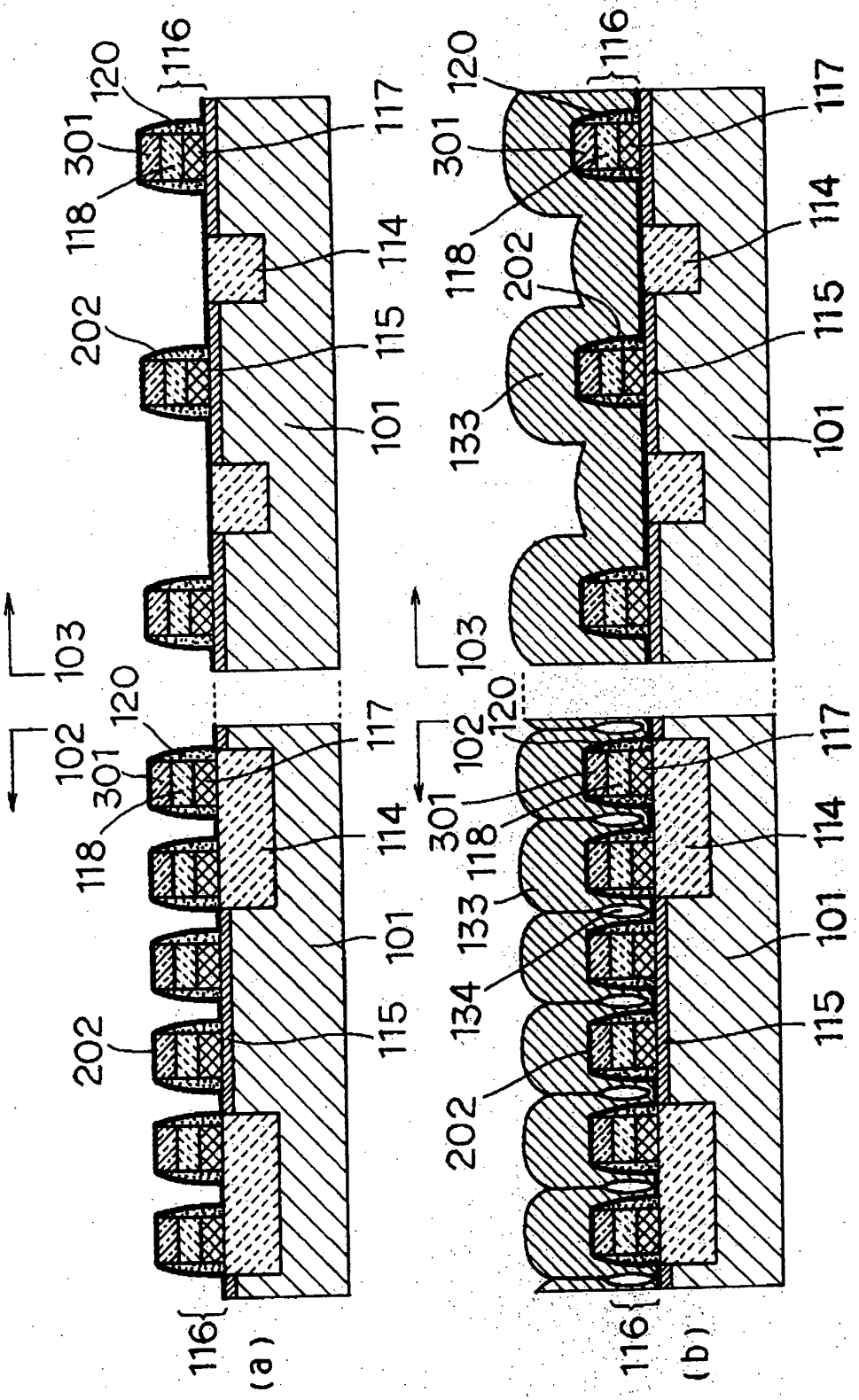
[Fig. 10]


300
301
120
202
116
117
114
133
101
115
123
103
102
112
118
110
113
111
121
122
NITRIDE PROTECTIVE FILM

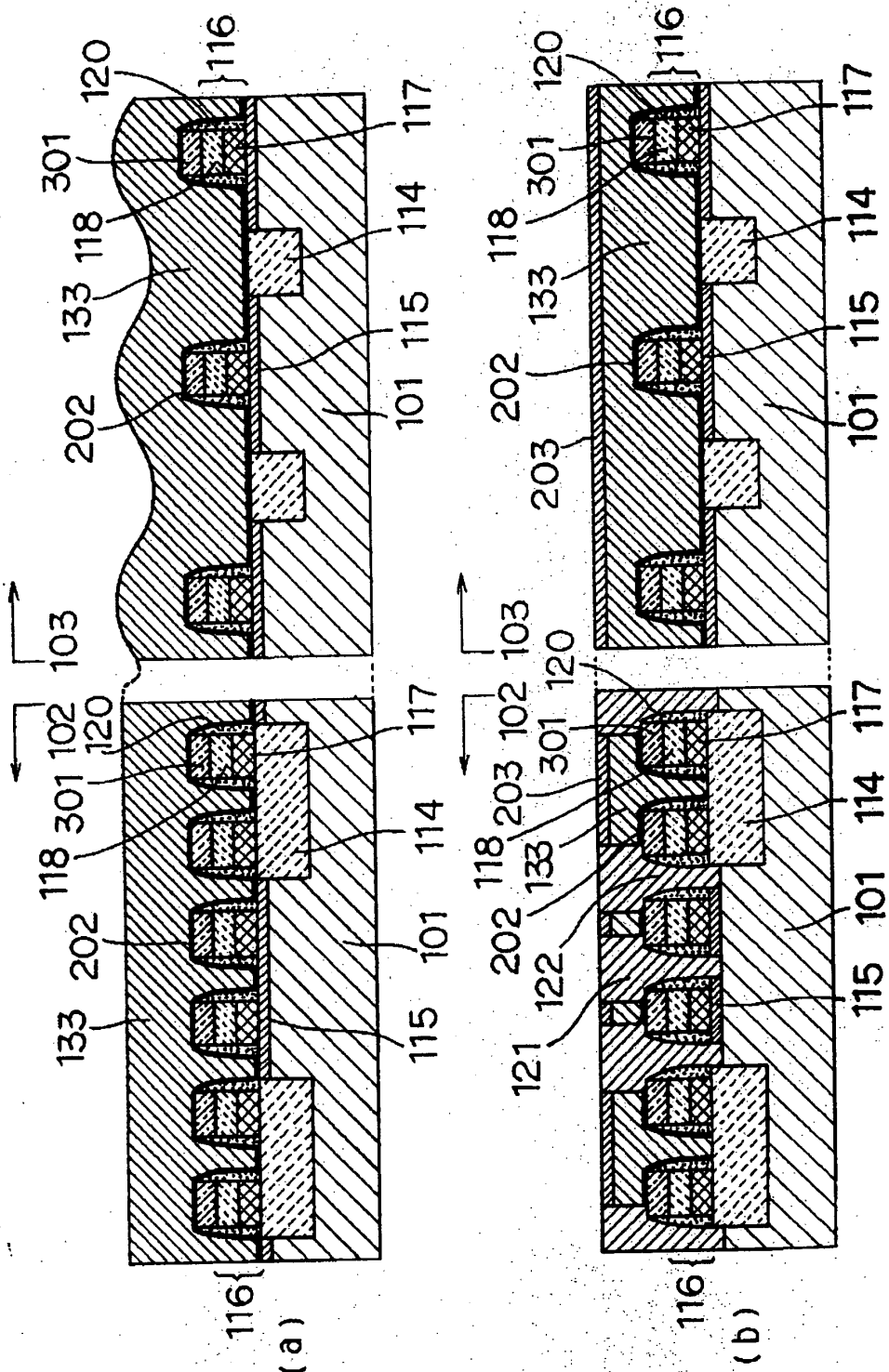
[Fig. 11]



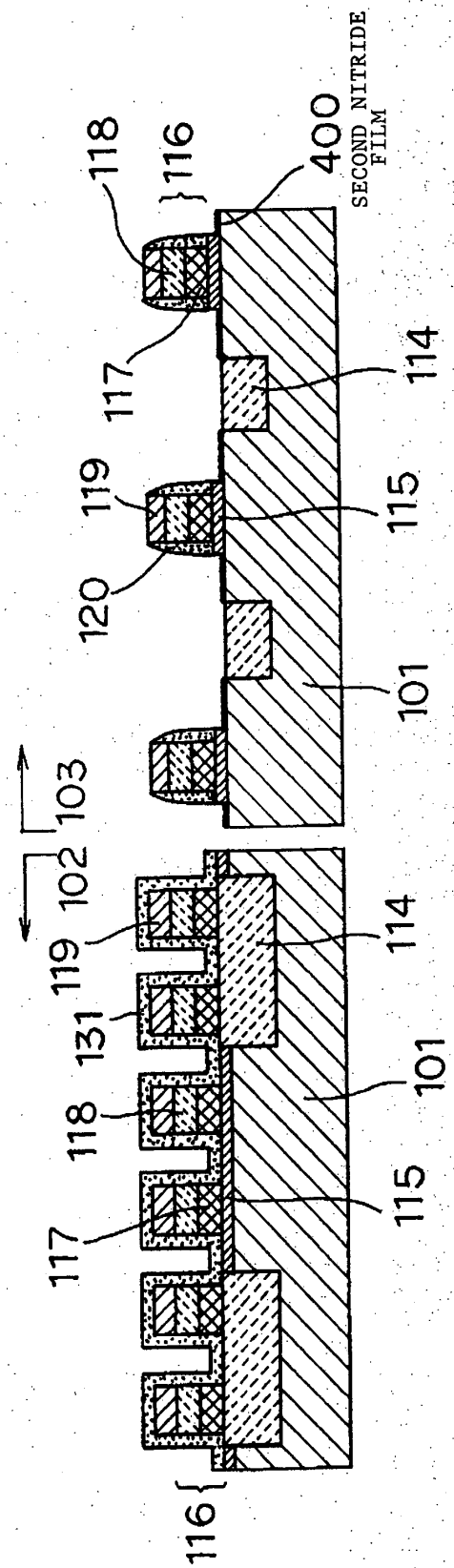
[Fig. 12]



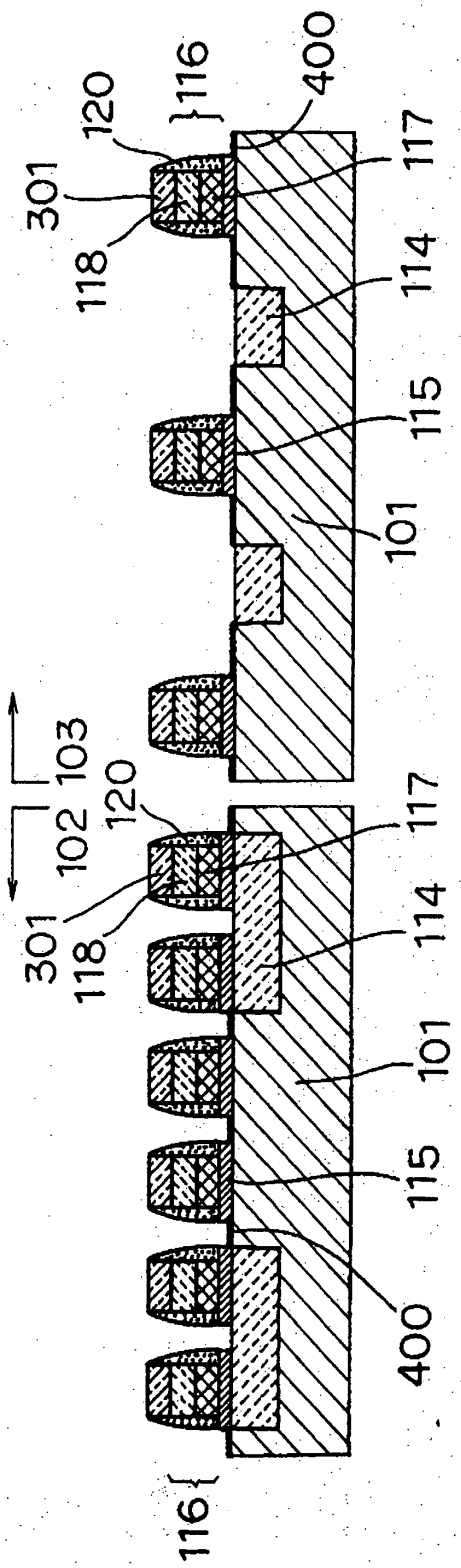
[Fig. 13]



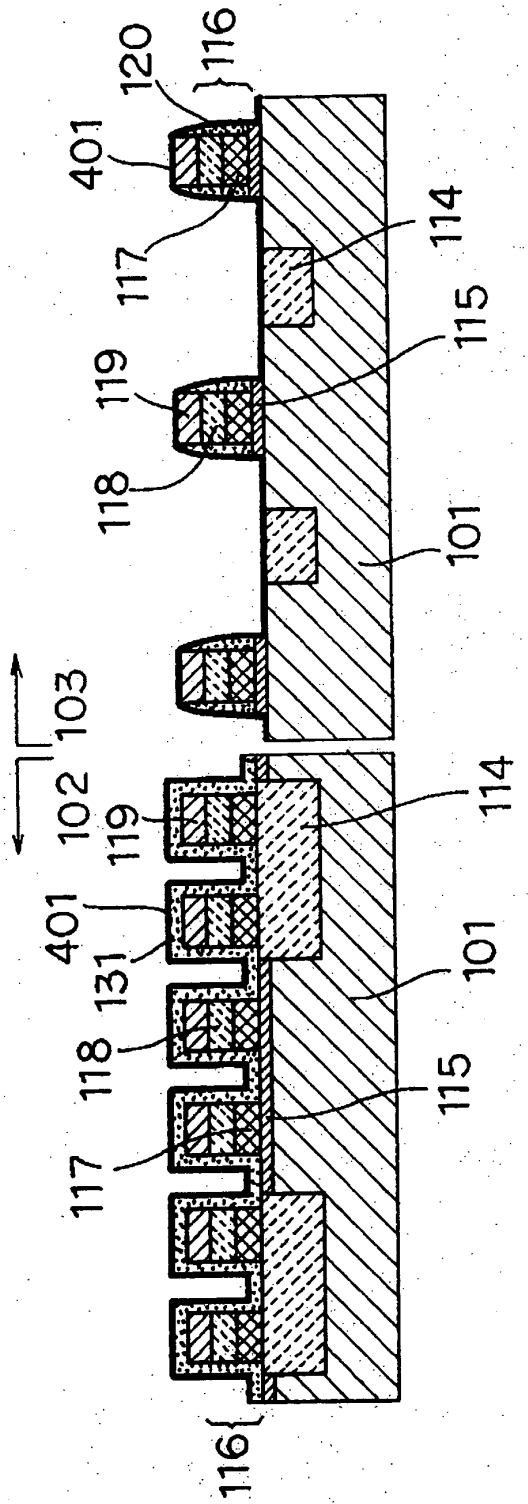
[Fig. 14]


400
SECOND NITRIDE FILM
118
116
117
114
119
115
120
101
103
102
119
114
131
101
118
115
117
116

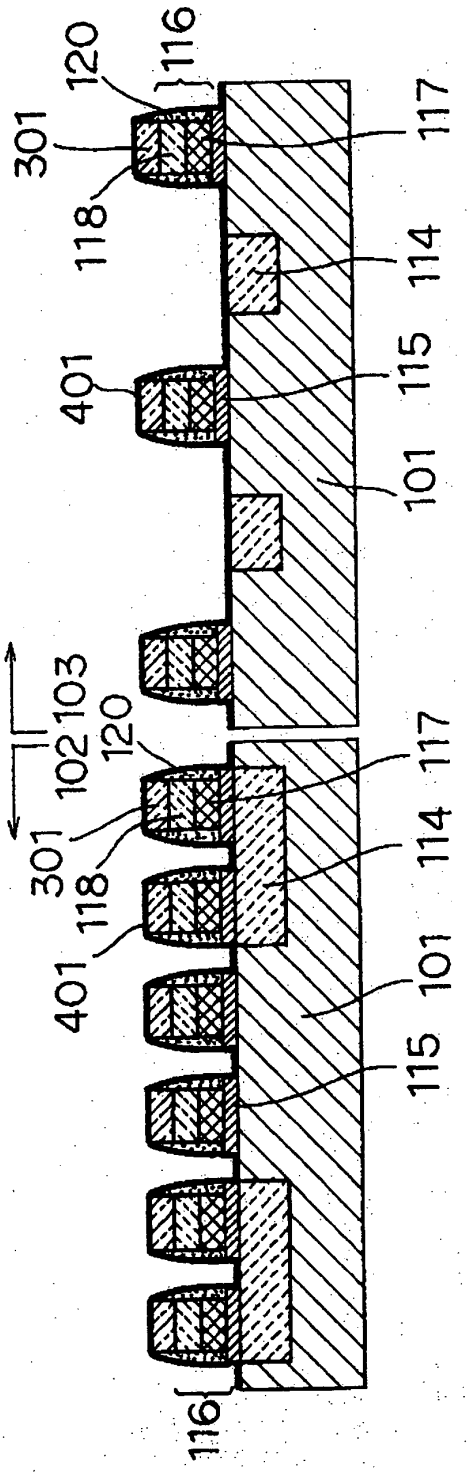
[Fig. 15]



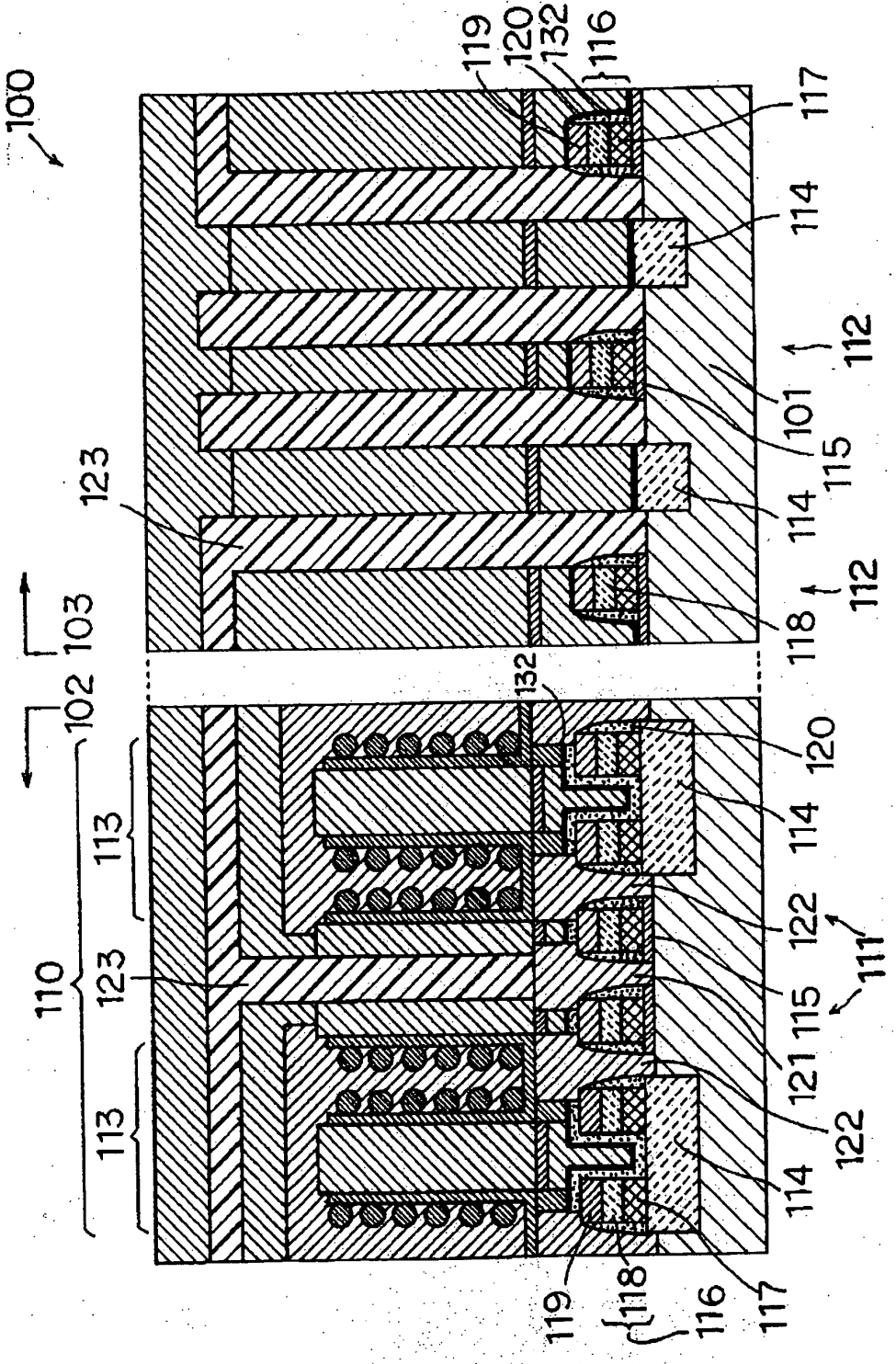
[Fig. 16]


120
116
401
117
114
115
119
118
101
103
102
119
114
401
131
101
118
115
117
116

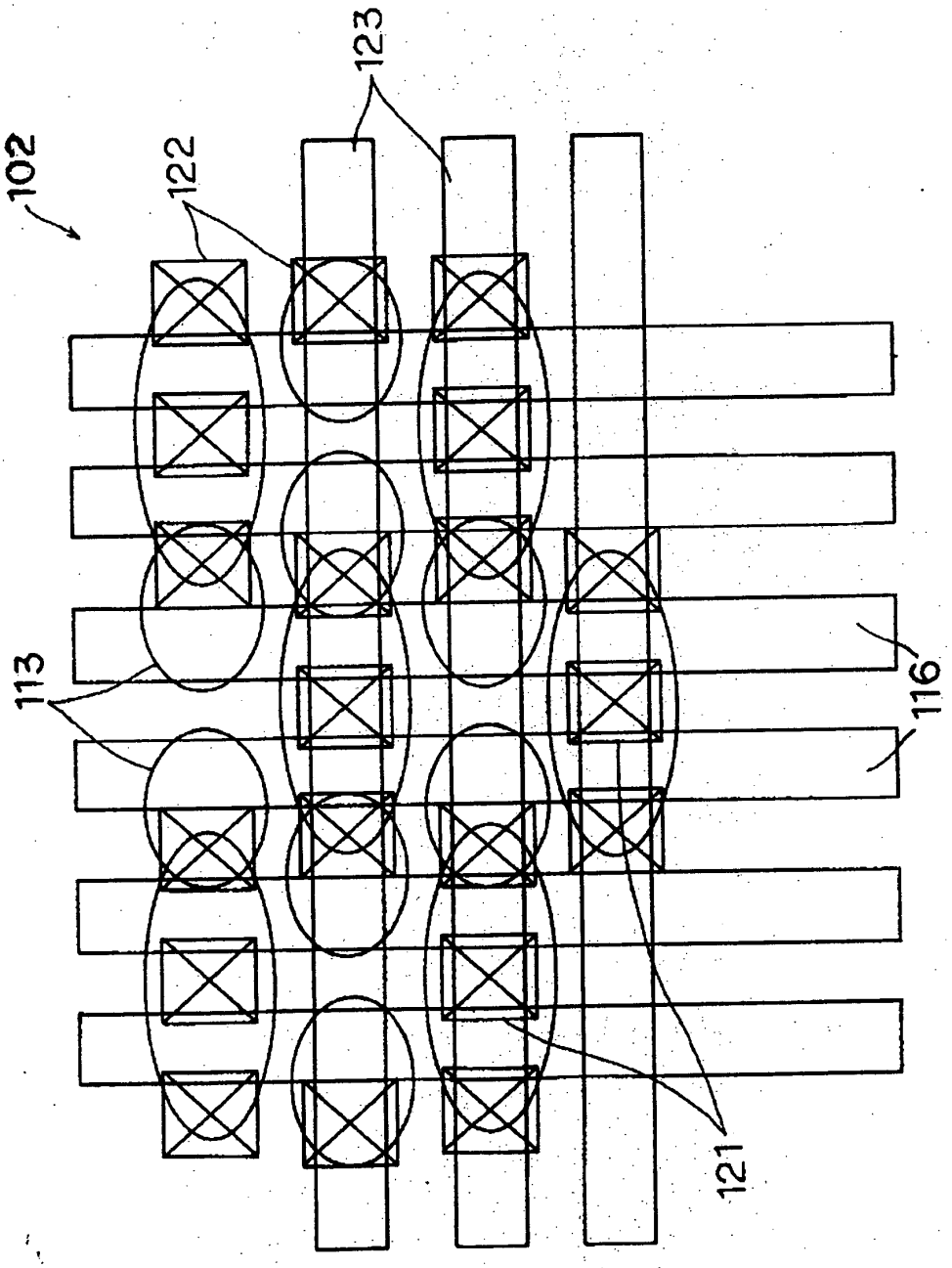
[Fig. 17]


120
116
301
117
118
114
401
115
101
103
102
120
117
301
114
118
401
101
115
116

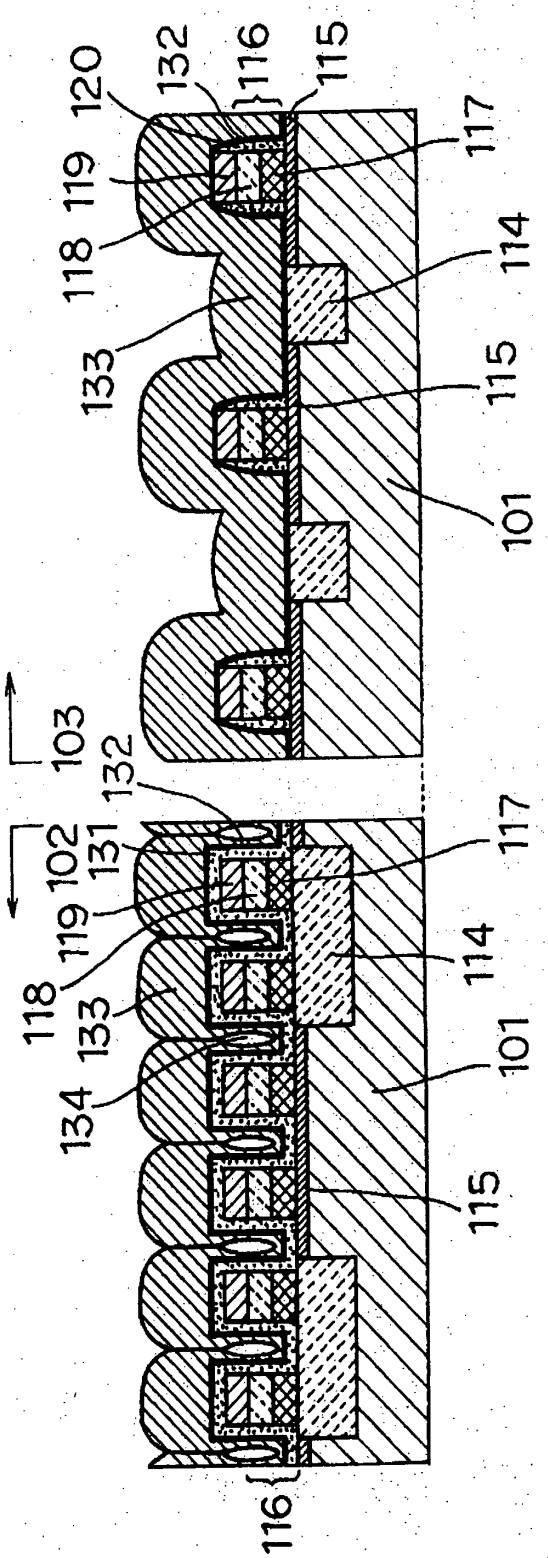
[Fig. 18]


100
119
120
132
116
117
114
112
101
115
123
103
102
118
113
110
111
121
122

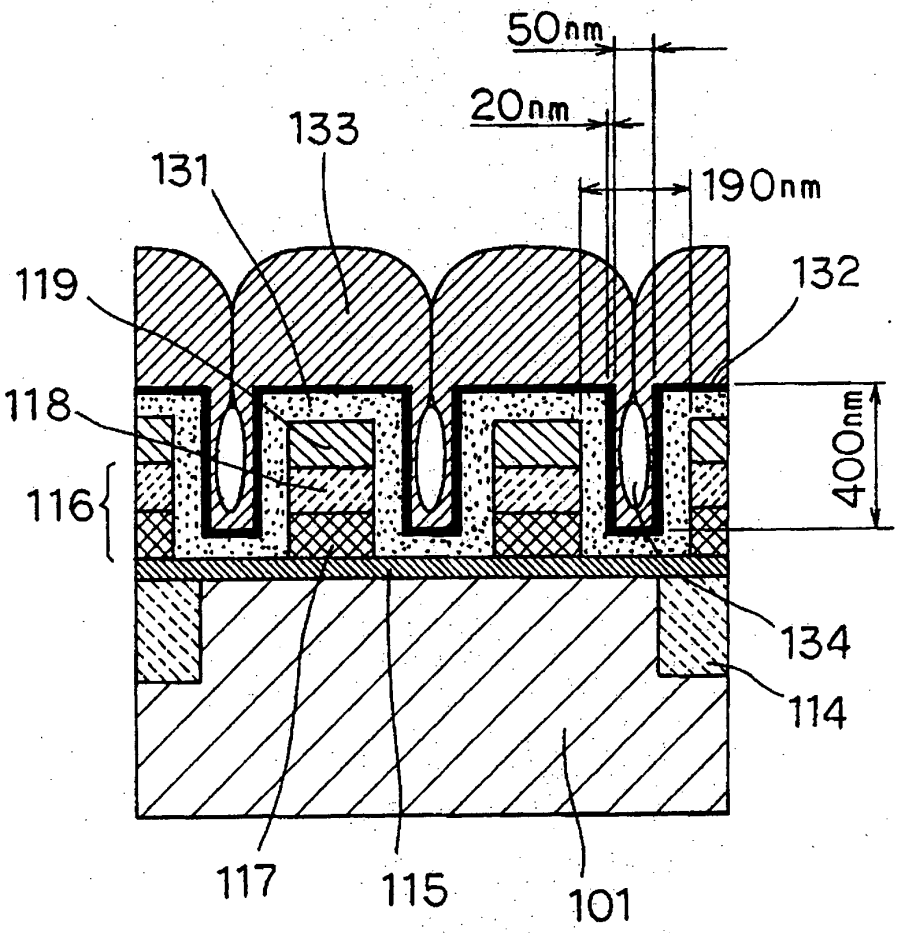
[Fig. 19]



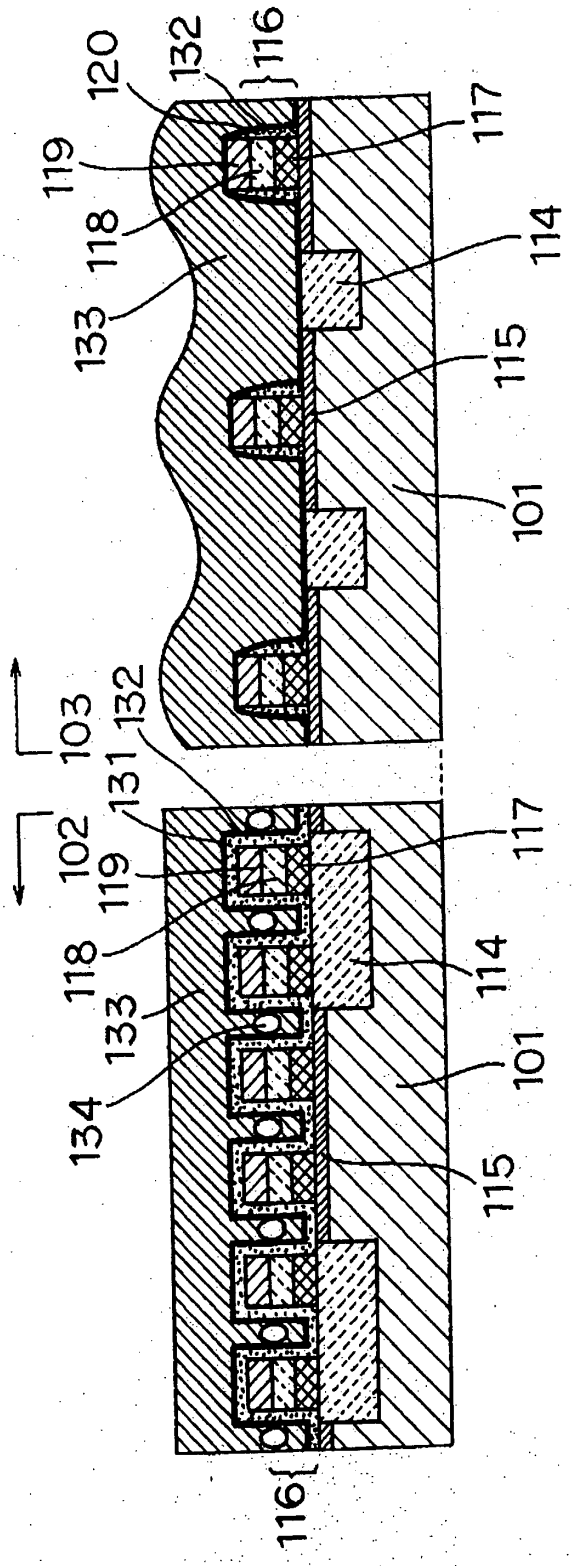
[Fig. 20]


120
132
116
115
117
119
118
114
133
115
101
103
132
102
131
117
119
114
118
133
101
134
115
116

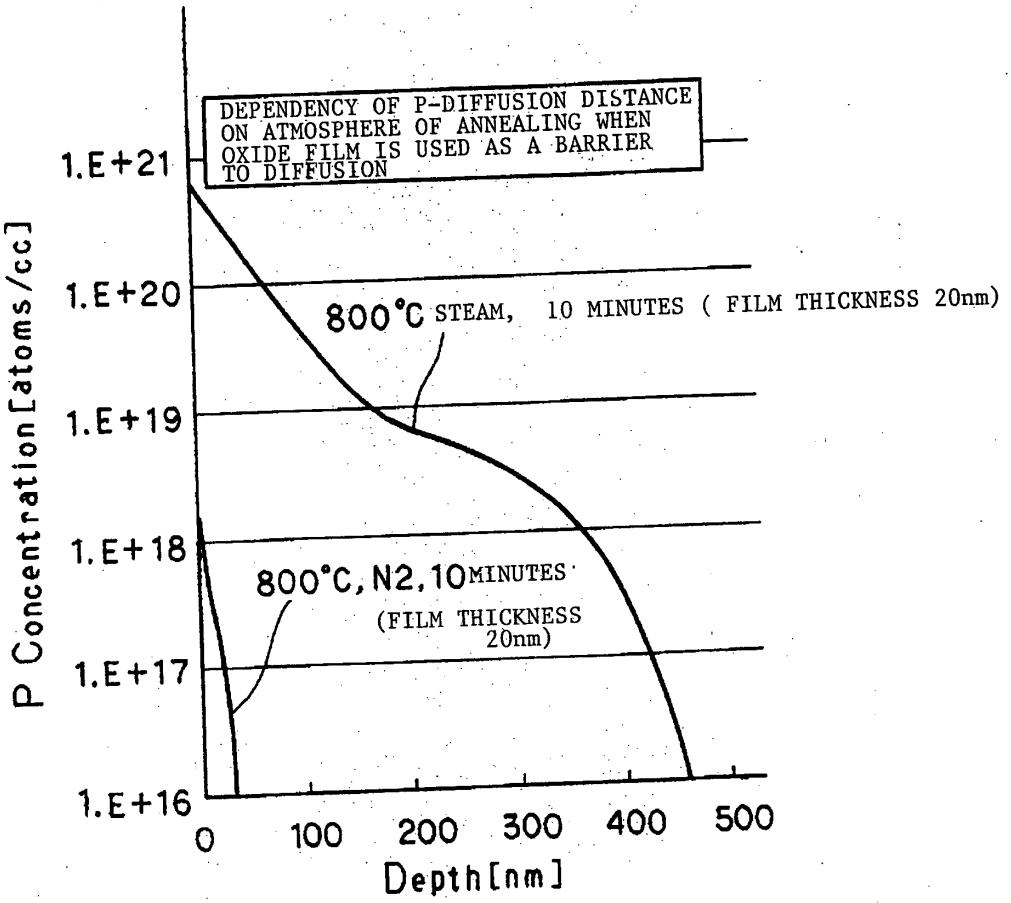
[Fig. 21]


50nm
20nm
190nm
133
131
119
132
118
116
400nm
134
114
117
115
101

[Fig. 22]


120
132
116
119
117
118
114
133
115
101
103
132
131
102
119
117
118
114
133
101
134
115
116

[Fig. 23]


DEPENDENCY OF P-DIFFUSION DISTANCE ON ATMOSPHERE OF ANNEALING WHEN OXIDE FILM IS USED AS A BARRIER TO DIFFUSION
800°C STEAM, 10 MINUTES (FILM THICKNESS 20nm)
800°C, N2, 10MINUTES
(FILM THICKNESS 20nm)
P Concentration [atoms/cc]
1.E+21
1.E+20
1.E+19
1.E+18
1.E+17
1.E+16
0
100
200
300
400
500
Depth [nm]

【Document Name】 Abstract

【Abstract】

【Problem】 To manufacture a DRAM having both of high- and low-density regions, and so on

【Means to Solve】 a gate oxide film 115 and gate electrodes 116 are formed on a surface of the semiconductor substrate 101, a first nitride film 131 is uniformly formed and only the low-density region 103 is etched, a second nitride film 202 is uniformly formed and an interlayer insulating film 133 is formed, voids are eliminated by water-vapor annealing, contact holes are formed in the interlayer insulating film by self-alignment using the first nitride film 131 as an etching stopper in the high-density region 102, contact electrodes 121,122, and so on are formed, and then the assembly is annealed by a forming gas to recover an interfacial level. Since the second nitride film 202 is positioned on the surface of the semiconductor substrate 101 in the low-density region 103, even water-vapor annealing is conducted, an impurity can be prevented from being diffused from the interlayer insulating film 133 into the semiconductor substrate 101 and the semiconductor substrate 101 can be prevented from being oxidized, but the second nitride film does not prevent the diffusion of the forming gas.

【Selected Figure】 FIG. 1